Lecture #4 Outline

- Announcements

- Project Proposal

- AVR Processor Resources

  - A/D Converter (Analog to Digital)

  - Analog Comparator

  - Real-Time clock using Timer 2

Announcements

- Lab#2 in progress

  - Due date: **Monday Oct 14, 5pm**

- Projects

  - Arrange to meet and discuss your ideas

  - Project Proposal: Due Friday Oct 25, 5pm

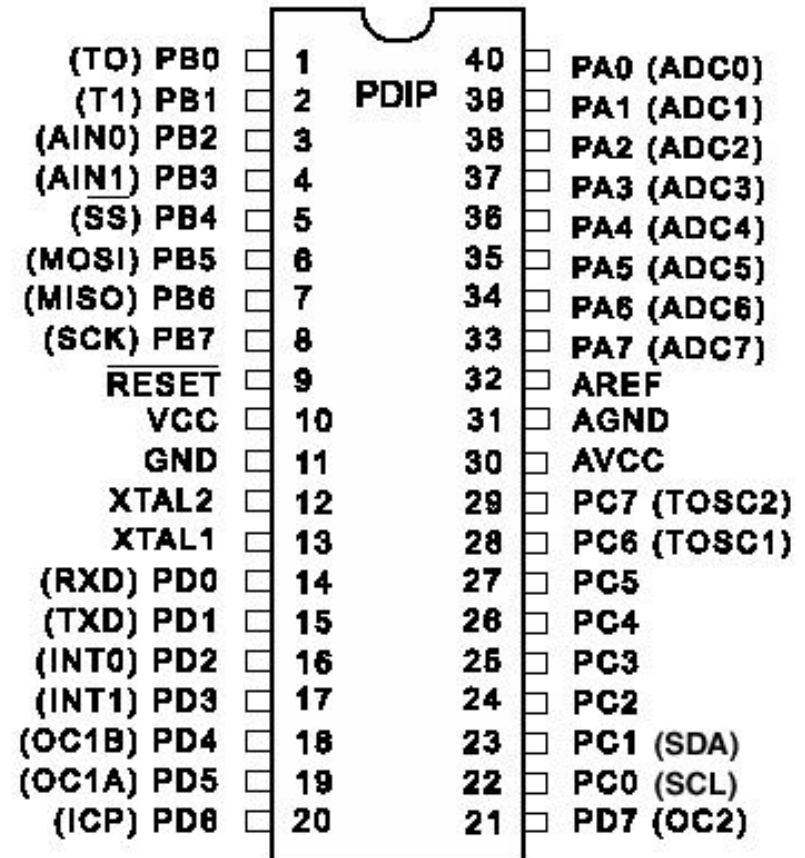# **Project Proposals**

- 1-2 page proposal including:
  - Name of your project
  - Team members
  - Project description
    - Be sure to cover **at least** what purpose your project serves, how you expect it to work or how someone will use it, how it will look (use graphics), how the user will interact with the project (inputs and outputs), what features of the AVR processor you intend to use, how you will write your code (asm, C, mixed), and how you will build you project (wire-wrap, perf-board, hand-soldered, case?)
  - List of important parts
    - Should include all major/critical parts or modules
    - List real part numbers, not just descriptions
    - Don't forget to include the AVR processor you intend to use
  - Areas in which you might need help

AVR Processor Resources

- Interrupts

- Timers

- UART (Universal Asynchronous Receiver/Transmitter)

- SPI (Serial Peripheral Interface)

- A/D Converters (Analog to Digital)

- Analog Comparator

EE281

Embedded System
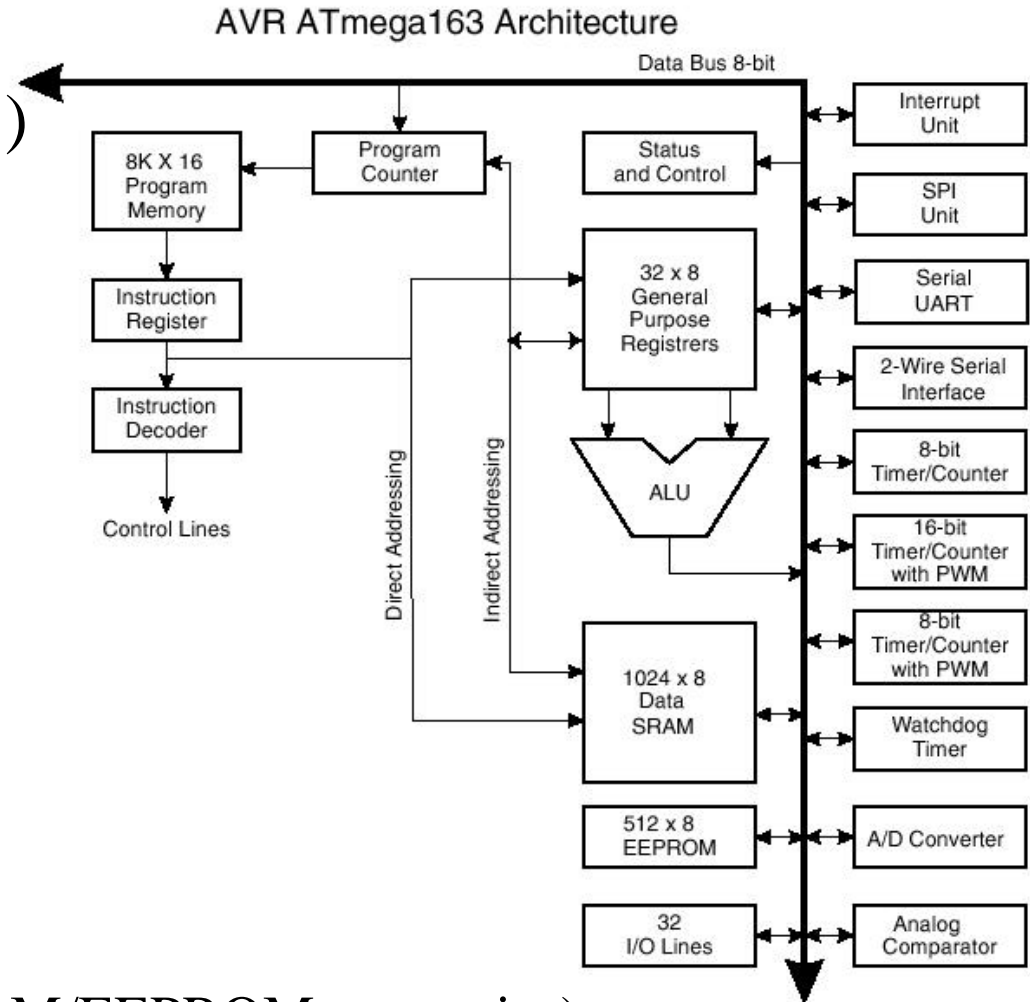Design Laboratory

- General Purpose Ports
  - PORTA (A/D conv)
  - PORTB
  - PORTC
  - PORTD
  - (Special Functions)
- Special Purpose Pins
  - Crystal (XTAL1/XTAL2)
  - Real Time Crystal (TOSC1/2)
  - RESET
  - AREF, AVCC, AGND
- Power (VCC/GND)

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              PDIP
(T0)  PB0  [ 1      40 ]  PA0 (ADC0)
(T1)  PB1  [ 2      39 ]  PA1 (ADC1)
(AIN0) PB2 [ 3      38 ]  PA2 (ADC2)
(AIN1) PB3 [ 4      37 ]  PA3 (ADC3)
(SS)  PB4  [ 5      36 ]  PA4 (ADC4)
(MOSI) PB5 [ 6      35 ]  PA5 (ADC5)
(MISO) PB6 [ 7      34 ]  PA6 (ADC6)
(SCK) PB7  [ 8      33 ]  PA7 (ADC7)
RESET      [ 9      32 ]  AREF
VCC        [ 10     31 ]  AGND
GND        [ 11     30 ]  AVCC
XTAL2      [ 12     29 ]  PC7 (TOSC2)
XTAL1      [ 13     28 ]  PC6 (TOSC1)
(RXD) PD0  [ 14     27 ]  PC5
(TXD) PD1  [ 15     26 ]  PC4
(INT0) PD2 [ 16     25 ]  PC3
(INT1) PD3 [ 17     24 ]  PC2
(OC1B) PD4 [ 18     23 ]  PC1 (SDA)
(OC1A) PD5 [ 19     22 ]  PC0 (SCL)
(ICP) PD6  [ 20     21 ]  PD7 (OC2)
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- 32 Registers (R0-R31)

- 8 Kw Prog ROM

- 1 Kb RAM

- 512 bytes EEPROM

- 32 I/O lines

- 18 Interrupts

- A/D Converter

- Timer 2

- I^{2}C Bus

(Mega323 doubles ROM/RAM/EEPROM memories)

AVR ATmega163 Architecture

Data Bus 8-bit

| 8K X 16 Program Memory | Program Counter | | Status and Control | | Interrupt Unit |

| Instruction Register | | | 32 x 8 General Purpose Registrers | | SPI Unit |

| Instruction Decoder | | | | | Serial UART |

| | | | ALU | | 2-Wire Serial Interface |

Control Lines

Direct Addressing   Indirect Addressing

8-bit Timer/Counter

16-bit Timer/Counter with PWM

1024 x 8 Data SRAM

8-bit Timer/Counter with PWM

Watchdog Timer

512 x 8 EEPROM

A/D Converter

32 I/O Lines

Analog Comparator

A/D Converters

- An A/D converter converts a sensed analog voltage into a binary value
  - Example: 0-5V might convert to 0-255 binary
- The mega163/323 A/D converters provide:
  - Successive-Approximation conversion
  - 8 channels (inputs)
  - 8, 9, or 10 bits resolution (1 LSB typical accuracy)
  - 65-260us conversion time
  - Single-conversion or Free-Running mode
  - Conversion Complete Interrupt

A/D Registers

- ADCH/ADCL (A/D Result Register)
  - Read the high and low portion of the conversion result from these registers

- ADCSR (A/D Control and Status Register)
  - A/D Enable bit
  - A/D Start Conversion bit
  - A/D mode select (single conversion or free-run)
  - Set A/D Converter clock rate (prescaler)
  - Interrupt Enable, Mask, and Flag bits

- ADMUX (A/D Multiplexer Register)
  - Select your input channel (input pin)
  - Select a voltage reference

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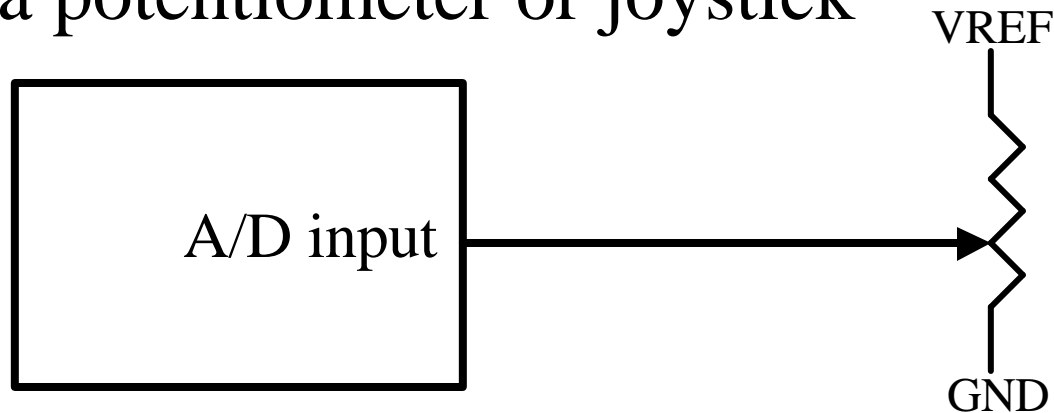Design Laboratory

Embedded System
Design Laboratory
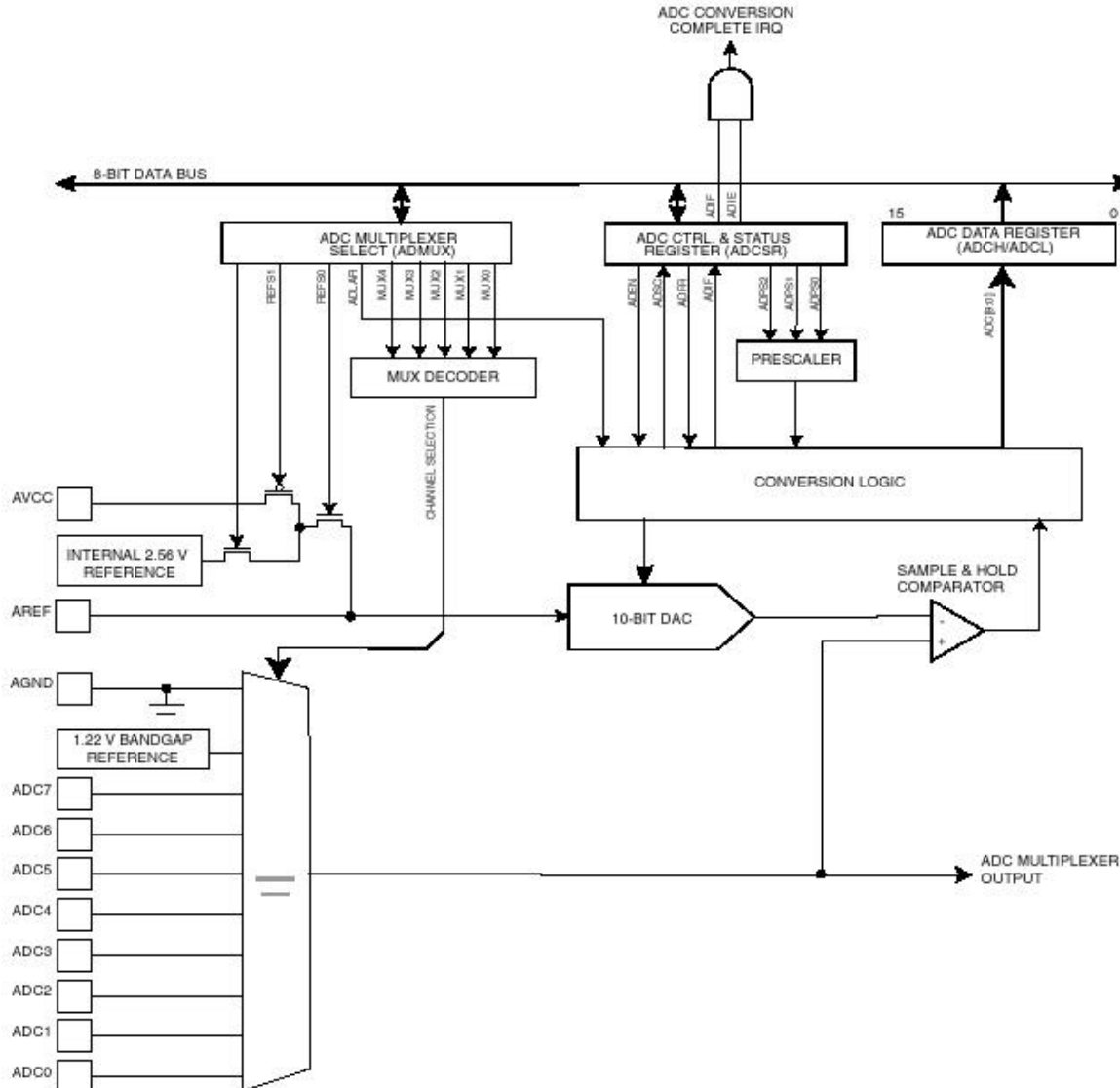
- Input ranges and VREF
  - A reference is required to make any measurement
  - VREF is the reference voltage against which A/D inputs are measured (internal 2.56V or external VREF pin)
  - Analog input range of the A/D converters is 0-VREF volts

- Output ranges
  - The output range is defined by the number of bits the A/D converter produces across its input range
    - 0-VREF → 8 bits → 0-255 (Resolution = VREF/256)
    - 0-VREF → 9 bits → 0-512 (Resolution = VREF/512)
    - 0-VREF → 10-bits → 0-1024 (Resolution = VREF/1024)

Example: VREF = 2.56V   Conv. output = 120

                  Voltage in was (120/256)*VREF = 1.2V

Embedded System
Design Laboratory

- With a potentiometer or joystick

VREF

A/D input

GND

- With a sensor

VREF

A/D input

GND
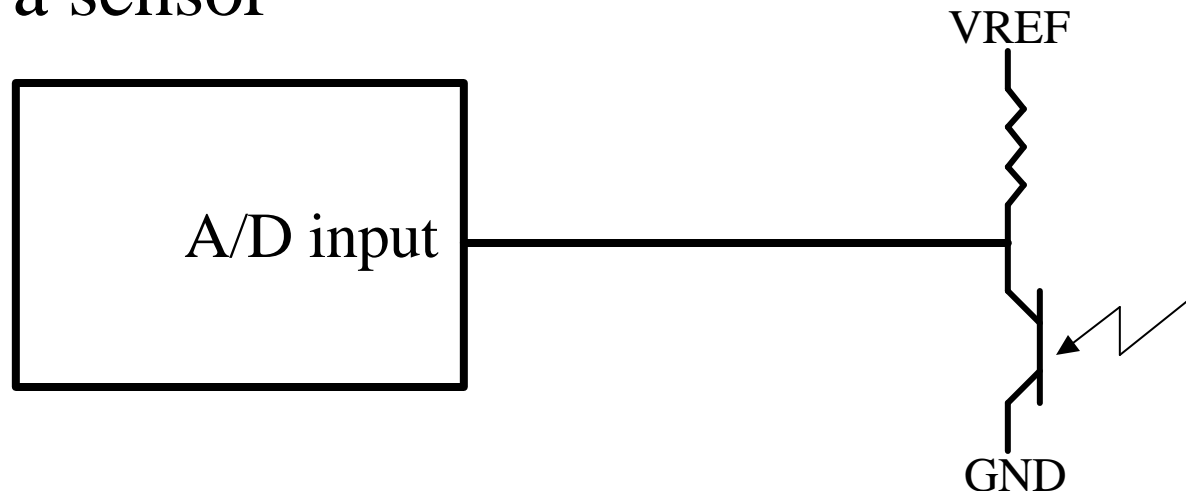
Analog Comparator

- Compares voltages on AIN0 and AIN1
- Reports which is greater
- Can trigger interrupt on:
  - AIN0 > AIN1
  - AIN0 < AIN1
  - Both
- ACSR (Analog Comparator Status Register)
  - Select source of input
  - Enable/Disable interrupt
  - Select interrupt condition

EE281

Embedded System
Design Laboratory

- Mega163/323 includes an extra 8-bit Timer 2

- Timer 2 is designed to be able to operate as a Real-Time Clock
  - Connect 32.768KHz crystal between TOSC1/2
  - Set Timer 2 prescaler to use external crystal as input
  - Set Prescaler division ratio to provide overflow at convenient intervals (like 1Hz)
  - Use the OVFL interrupt service routine to keep track of time in ordinary HH:MM:SS