Midterm—“Extra Points”

1. A wave pipelined system has two registered segments. Suppose $C = 1$ nsec and clock skew is ±0.5 nsec. We have the following pipeline:

\[
\begin{array}{cc}
P_{\text{max}} = 7 & P_{\text{max}} = 5 \\
P_{\text{min}} = 4 & P_{\text{min}} = 4 \\
0 & 1 & 2
\end{array}
\]

There is no clock skew at the origin “0.” What is the best cycle time?

$\Delta t =$ ______ nsec.

The constructive clock skew at “1” is ______ nsec.

The constructive clock skew at “2” is ______ nsec.

2. (a) If a certain $M/M/1$ open queue server is idle 25% of the time, what is its expected queue size? ______.

(b) For the server in (a), what buffer size should be used to ensure that overflow occurs for no more than 2% of the requested items? ______.

(c) When the buffer size is two entries, new requests are to be routed to other servers. This occurs with what frequency (probability)? ______.
3. A certain D-cache memory system has 4 modules, $T_c = 2$ cycles. The processor makes 0.3 DR and 0.15 DW requests each cycle. The writes are not buffered.

$$n = \_, \delta = \_, B(m, n, \delta) = \_.$$  

Now the writes are fully buffered so only the reads can slow the processor down. The mean queue total size for writes is \_. What is $Tw$ for writes? \_.

4. A superscalar processor is to have an interleaved D-cache with 4 LS/ST units. Each unit has a mean request rate of .5 requests per cycle. The cache module takes 2 cycles to complete an access and can be designed either as a two cycle module (one request each 2 cycles) or fully pipelined module (with one request each cycle).

(a) The first design (non-pipelined) has 8 modules; $n = \_, \delta = \_, B(m, n, \delta) = \_, Tw = \_\_\_\_\_ cycles, Perf_{rel} = \_.$

(b) The second design (pipelined) has 4 modules; $n = \_, \delta = \_, B(m, n, \delta) = \_, Tw = \_\_\_\_\_ cycles, Perf_{rel} = \_.$