CMOS Operational Amplifier Design and Optimization via Geometric Programming

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Abstract— **We describe a general method for optimized design of CMOS operational amplifiers. We observe that a wide variety of design objectives and constraints have a special form, *i.e.*, they are *posynomial* functions of the design variables. As a result, the amplifier design problem can be expressed as a special form of optimization problem called *geometric programming,* for which very efficient global optimization methods have been developed. As a consequence, we can efficiently determine *globally optimal* amplifier designs, or globally optimal tradeoffs between competing performance measures such as power, open-loop gain, and bandwidth. Our method, therefore, yields completely automated synthesis of (globally) optimal CMOS amplifiers, directly from specifications.**

In this paper, we apply this method to a specific common two-stage amplifier architecture. We compute globally optimal tradeoff curves relating performance measures such as power dissipation, crossover frequency, and open-loop gain.

I. Introduction

Operational amplifiers (op-amps) are an essential block of many analog systems. Due to increased interest in mixed mode integrated circuits, op-amps in CMOS technology have become very popular.

Performance of an op-amp is measured by several parameters such as open-loop voltage gain, quiescent power, input referred noise, output voltage swing, crossover frequency, input offset voltage, slew rate, and die area. Determining the optimal dimensions of the transistors for a specific design involves a tradeoff among all these performance measures. Since circuit specifications vary from system to system, one needs a custom design each time.

In this paper, we show how CMOS op-amp design can be posed as very special type of optimization problem called geometric programming. Recently developed algorithms can be used to compute very efficiently the global optimal solution of geometric programs, even when there are hundreds of variables and many hundreds, or thousands, of constraints. Thus, even challenging amplifier design problems with many variables and constraints can be globally solved. The method we present can be applied to a wide variety of amplifier architectures, but in this paper we apply the method to a specific two-stage amplifier architecture.

In Section II, we briefly describe geometric programming. In Section III, we describe a variety of performance measures and constraints involved in an op-amp design, and show that they have the required form for geometric programming. In Section IV, we discuss results and optimal trade-off curves for specific op-amp designs. Finally, in Section V we describe some extensions of the method.

II. Geometric Programming

Many design problems involve the minimization of an objective function subject to multiple constraints. There are many algorithms for numerically solving general optimization problems, but they share some common disadvantages. One is that they find points that are only *locally optimal*, not globally optimal. The usual approach to a global solution consists in minimizing many different initial designs and taking the best final design. This does not guarantee that the globally optimal design has been found. There are several methods that can be used to find globally optimal designs, but all have disadvantages. For instance, branch and bound methods involve many orders of magnitude more computation for small problems, and are generally intractable for medium or large scale problems.

There is an important class of optimization problems for which globally optimal solutions can be efficiently computed, even for large scale problems: convex optimization problems, in which the objective function and constraint set are convex [1]. Geometric programming is one of them.

Let f be a real-valued function of n real, positive variables $x = (x_1, x_2, \ldots, x_n)$. It is called a *posynomial* function if it has the form

$$f(x_1, \ldots, x_n) = \sum_{k=1}^{t} c_k x_1^{\alpha_{1k}} x_2^{\alpha_{2k}} \cdots x_n^{\alpha_{nk}}$$

where $c_j \geq 0$ and $\alpha_{ij} \in \Re$.When there is only one term in the sum, *i.e.*, $t = 1$, f is called a *monomial* function. Note that posynomials are closed under sums, products, and nonnegative scaling.

A *geometric program* has the form

$$\begin{array}{lll} \text{minimize} & f_0(x) & \\ \text{subject to} & f_i(x) \leq 1, & i = 1, \ldots, m \\ & g_i(x) = 1, & i = 1, \ldots, p \\ & x_i > 0, & i = 1, \ldots, n \end{array}$$

where f_i are posynomial functions and g_i are monomial functions. (See, *e.g.*, [2].)

In general, posynomial functions are not convex, so a geometric program is not a convex program. But a simple change of variables can be used to convert it to a convex program. We define new variables $y_i = \log x_i$, and take the logarithm of a posynomial f to get

$$h(y) = \log\left(f\left(e^{y_1}, \ldots, e^{y_n}\right)\right) = \log\left(\sum_{k}^{t} e^{a_k^T y + b_k}\right)$$

where $a_k^T = [\alpha_{1k} \cdots \alpha_{nk}]$ and $b_k = \log c_k$. It can be shown that h is a *convex* function of the new variable y. We can convert a standard geometric program into a convex program by expressing it as

$$\begin{array}{rll} \text{minimize} & \log f_0(e^{y_1}, \ldots, e^{y_n}) & \\ \text{subject to} & \log f_i(e^{y_1}, \ldots, e^{y_n}) \leq 0, & i = 1, \ldots, m \\ & \log g_i(e^{y_1}, \ldots, e^{y_n}) = 0, & i = 1, \ldots, p. \end{array}$$

This is the so-called exponential form of the geometric program, which can be solved using sophisticated new interior-point methods for nonlinear convex programming [4].

To carry out the designs in this paper, we implemented a simple primal barrier method for solving the exponential form of geometric programming [1]. For larger problems, more sophisticated interior-point methods for geometric programming have recently been developed, *e.g.* [3].

III. Two Stage CMOS Operational Amplifier

In this section we express the performance measures and design constraints for a specific op-amp configuration in terms of the design parameters: the transistor dimensions, the compensating capacitor value, and the bias current.

One of the most widely used topologies in CMOS op-amp implementation is shown in Figure 1. The circuit consists of an input differential stage driving an active load followed by a common-source stage also driving an active load. The feed-forward signal path through the compensating capacitor creates a zero in the right half plane. Stability can be improved by placing a resistor in series with the compensating capacitor [5].

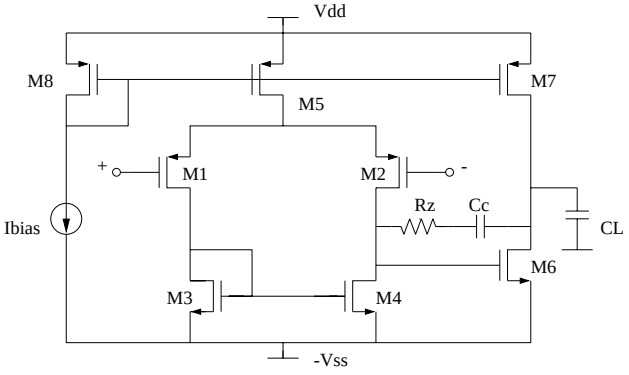

Fig. 1. Two stage operational amplifier

In deriving the design equations [5], we assume the transistors are long channel, square-law devices with

$$\begin{array}{rcl} \text{transconductance} & \triangleq & g_m = \sqrt{2 I_D \mu C_{ox} \dfrac{W}{L}} \\ \text{output conductance} & \triangleq & g_o = \lambda I_D. \end{array}$$

- Power Dissipation

$$P = V_{\rm dd}\left(I_{\rm bias} + I_5 + I_7\right) = V_{\rm dd} I_{\rm bias}\left(1 + \frac{L_8 W_5}{W_8 L_5} + \frac{L_8 W_7}{W_8 L_7}\right)$$

Note that P is a posynomial function of the design parameters.

- Open Loop Voltage Gain

Assuming that M_1 and M_2 are identical and that M_3 and M_4 are identical, the gain can be shown to be

$$A_v = \left(\frac{g_{\rm m_2}}{g_{\rm o_2} + g_{\rm o_4}}\right)\left(\frac{g_{\rm m_6}}{g_{\rm o_6} + g_{\rm o_7}}\right).$$

Note that the gain is a monomial function of the design parameters. Thus we can impose a constraint that requires the gain to be *equal* to a certain required value.

- Systematic Input Offset Voltage

In order to reduce the input offset voltage, the drain voltage of M_3 and M_4 must be equal. This condition occurs when

$$\frac{(W/L)_3}{(W/L)_6} = \frac{(W/L)_4}{(W/L)_6} = \frac{1}{2}\frac{(W/L)_5}{(W/L)_7}.$$

Note that these conditions are all equality constraints involving monomials, hence readily handled by geometric programming.

- Input-Referred Noise

Assuming that $g_{\rm m_1} = g_{\rm m_2}$ and $g_{\rm m_3} = g_{\rm m_4}$, input referred noise can be expressed as the sum of the input referred $1/f$ noise and the input referred thermal noise by

$$\begin{aligned} \frac{v_{in}^2}{\Delta f} &= \frac{2K_p}{C_{\rm ox} W_1 L_1}\left(1 + \frac{K_n \mu_{\rm n} L_1^2}{K_p \mu_{\rm p} L_3^2}\right)\frac{1}{f} \\ &\quad + \frac{16KT}{3\sqrt{2\mu_{\rm p} C_{\rm ox}(W/L)_1 I_1}}\left(1 + \sqrt{\frac{\mu_{\rm n}(W/L)_3}{\mu_{\rm p}(W/L)_1}}\right). \end{aligned}$$

This, too, is a (complicated) posynomial function of the design parameters (and f as well).

- Frequency Compensation

The circuit without the feedforward resistor has two poles and one zero which are located approximately at

$$p_1 \approx \frac{-g_{\rm m_1}}{A_{\rm v} C_{\rm c}} \qquad p_2 \approx \frac{-g_{\rm m_6}}{C_{\rm L}} \qquad z_1 \approx \frac{g_{\rm m_6}}{C_{\rm c}}.$$

In a typical design, p_1 is made the dominant pole. For unity feedback stability, the phase shift from the other poles and zeros at the unity gain bandwidth cannot exceed 90° minus the required phase margin. In the case of a dominant pole, the unity gain bandwidth is approximately

$$\omega_{\rm c} \approx \frac{g_{\rm m_1}}{C_{\rm c}}.$$

and the condition for stability becomes

$$\frac{\omega_{\rm c}}{p_2} + \frac{\omega_{\rm c}}{z_1} \leq \frac{\pi}{2} - {\rm PM}$$

where PM is the required phase margin and where we have assumed that for small phase shifts, $\tan^{-1}(x) \approx x$. Note that this phase margin constraint is posynomial in the design parameters, since ω_c, p_2, and z_1 are monomials in the design parameters.

A nulling resistor of value $1/g_{\rm m_6}$ in series with the compensating capacitor moves the zero to infinity. If the resistor

is of value $\frac{1}{g_{m_6}} \cdot \left(1 + \frac{C_L}{C_c}\right)$ the zero is moved to cancel p_2. The nulling resistor introduces a new pole located at

$$p_3 \approx \frac{-g_{m_3}}{C_1}$$

where C_1 is the equivalent capacitance at the gate of M_6. With the nulling resistor the phase margin constraint is also posynomial.

- Output Voltage Swing

The output voltage swing is determined transistor by M_6 and M_7 entering the linear region, *i.e.*,

$$\begin{aligned} \sqrt{\frac{I_6 L_6}{\mu_n C_{ox}/2W_6}} &\leq V_{out} \\ \sqrt{\frac{I_7 L_7}{\mu_p C_{ox}/2W_7}} + V_{out} &\leq V_{dd}. \end{aligned}$$

These constraints are posynomial inequalities in the design variables and the extra variable V_{out}.

- Area

The op-amp area can be approximated by

$$\text{Area} = \alpha_1 C_c + \alpha_2 \sum_i W_i L_i$$

where α_1 is a constant and α_2 accounts for wiring area. The area is thus posynomial in the design parameters.

- Minimum Device Sizes

$$L_i \geq L_{min} \qquad W_i \geq W_{min}.$$

These constraints are evidently the posynomial inequalities $L_{min}/L_i \leq 1$, $W_{min}/W_i \leq 1$.

- Common mode Input Range

The common mode input voltage is upper-bounded by M_5 entering the linear region and lower-bounded by M_3 and M_4 entering the linear region, *i.e.*,

$$\begin{aligned} \sqrt{\frac{I_1 L_1}{\mu_p C_{ox}/2W_1}} + \sqrt{\frac{I_5 L_5}{\mu_p C_{ox}/2W_1}} &\leq V_{dd} - V_{cm} + V_{TP} \\ \sqrt{\frac{I_3 L_3}{\mu_n C_{ox}/2W_3}} &\leq V_{cm} - V_{TP} - V_{TN}. \end{aligned}$$

We can impose a minimum common mode input range.

- Slew Rate

$$\text{SR} = \frac{I_1 \omega_u}{g_{m_1}} = \frac{I_1}{C_c}.$$

Thus, SR is a monomial function.

- Symmetry and Matching

Transistors M_1 and M_2 are identical and transistors M_3 and M_4 are identical. Biasing transistors (M_5, M_7 and M_8) have the same length for matching reasons, *i.e.*,

$$\begin{aligned} W_1 &= W_2 \qquad & L_1 &= L_2 \\ W_3 &= W_4 \qquad & L_3 &= L_4. \\ & & L_5 &= L_7 = L_8. \end{aligned}$$

These equality constraints can be written as monomial equalities, *e.g.*,$W_1/W_2 = 1$.

- Common Mode Rejection Ratio

$$\text{CMRR} = \frac{2 g_{m_1} g_{m_3}}{(g_{o_3} + g_{o_1})\, g_{o_5}}.$$

Note the CMRR is a monomial function.

- Bias Conditions

Each transistor must be in saturation. A bias constraint for each transistor must therefore be included.

IV. Optimization results

Since all the op-amp performance measures and constraints shown above can be expressed as posynomial functions, we can solve a wide variety of op-amp design problems via geometric programming. We can, for example, maximize the bandwidth subject to given (upper) limits on op-amp power, area, phase margin, and input offset voltage, and given (lower) limits on transistor lengths and widths, and op-amp voltage gain, CMRR, slew rate, and output voltage swing. The resulting optimization problem is evidently a geometric programming problem. The problem may appear to be very complex, involving many complicated inequality and equality constraints, but in fact is readily solved in seconds (or less). Moreover, the solution found is the *global* optimum, meaning that no design method of any kind can do better. If the constraints are infeasible, meaning that they cannot be simultaneously satisfied, then the solution algorithm terminates, announcing that infeasibility has been determined. By repeatedly solving optimal design problems as we sweep over values of some of the constraint limits, we can sweep out globally optimal tradeoff curves for the op-amp.

In this section, we present the results obtained for different designs. A 1.2μm CMOS technology with oxide thickness 20nm, NMOS threshold voltage of 0.7V, and PMOS threshold voltage of -0.9V was used. Common mode input voltage was fixed at half the supply. The output voltage ranged from 0.5V to 0.5V below the supply . The load capacitance was held constant at 3pF. Supply voltage was 5V, phase margin was $\geq 60°$, and gain was ≥ 10kV/V.

In the first experiment, we compare the results of cancelling the feedforward zero with the nulling resistor to the results of cancelling the second dominant pole. Figure 2 shows the two globally optimal tradeoff curves for crossover frequency versus power.

In all the experiments to follow, the nulling resistor is used to cancel the second dominant pole. A second experiment compared the maximum unity gain bandwidth versus power for different supply voltages. The results can be seen in Figure 3. Notice maximum bandwidth is obtained with large supply voltage and power. However, if a low power design is desired, lower supply voltages provide a larger unity gain bandwidth.

In a third experiment, we found the maximum unity gain bandwidth versus power for different open-loop gains. The optimal trade-off curve is plotted in Figure 4. Observe that when power is not limited, larger bandwidths can be

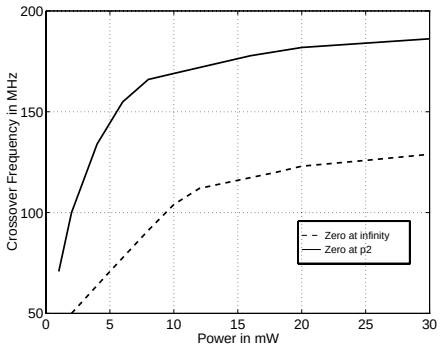

Fig. 2. Unity gain bandwidth vs. power for different nulling resistors

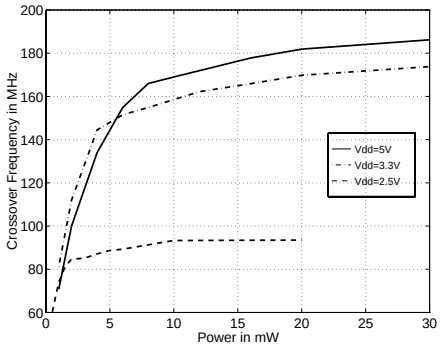

Fig. 3. Unity gain bandwidth vs. power for different supply voltages

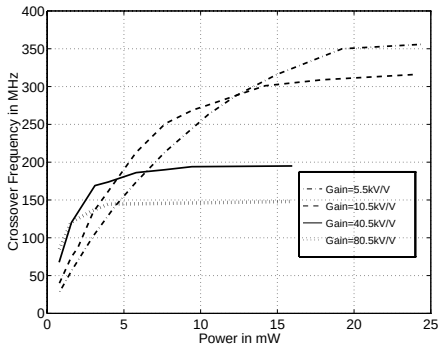

Fig. 4. Unity gain bandwidth vs. power for different open-loop gains

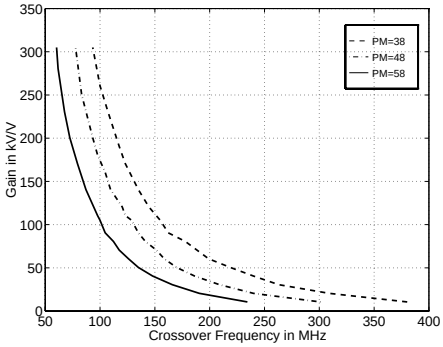

Fig. 5. Unity gain bandwidth vs. gain for different phase margins

obtained with smaller gains. The situation is inverted when there is a tight power budget. In this case, higher gains yield higher unity gain bandwidth.

In a fourth experiment, the optimal tradeoff curve (Figure 5) between open-loop gain and unity gain bandwidth was found. A generous power budget of 200mW was chosen.

V. Extensions

Other constraints that can be handled include robustness to process variation. This is done by repeating constraints for different process parameters. The additional constraints ensure circuit operation under various processing conditions.

The simple square-law equations have limited accuracy. Moreover, if more accurate models are used, we are likely to lose the special posynomial form of the constraints that is the basis of our method. Therefore, our claim of global optimality has to be qualified: we mean globally optimal for the square-law model equations we use. The first implication is that all designs that come from our geometric programming method must be checked by, for example, SPICE simulation with detailed, accurate models, to verify that the actual gain, bandwidth, power, and so on are close to the ones predicted by the posynomial formulas. (We have done that for a variety of designs from the tradeoff curves shown; in all cases our designs were verified.) It is also possible to follow the geometric programming design with a local optimization method that uses non-posynomial but more accurate model equations. Thus, the geometric programming method is used to get close to the optimal point, and the final design is tuned using the more accurate (but non-posynomial) model equations.

VI. Conclusions

We have presented a general method for designing and optimizing CMOS operational amplifiers. The method consists of expressing the op-amp design problem as a geometric program. Most op-amp performance measures and constraints are shown to be posynomial functions. A globally optimal solution can be efficiently computed for each specific case. The program executes quickly and therefore, automatic optimal op-amp design, directly from specifications, becomes an attractive possibility.

VII. Acknowledgments

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