OPERA: OPtimization with Ellipsoidal uncertainty for Robust Analog IC design

Yang Xu, Kan-Lin Hsiung, Xin Li
Ivan Nausieda, Stephen Boyd, Larry Pileggi

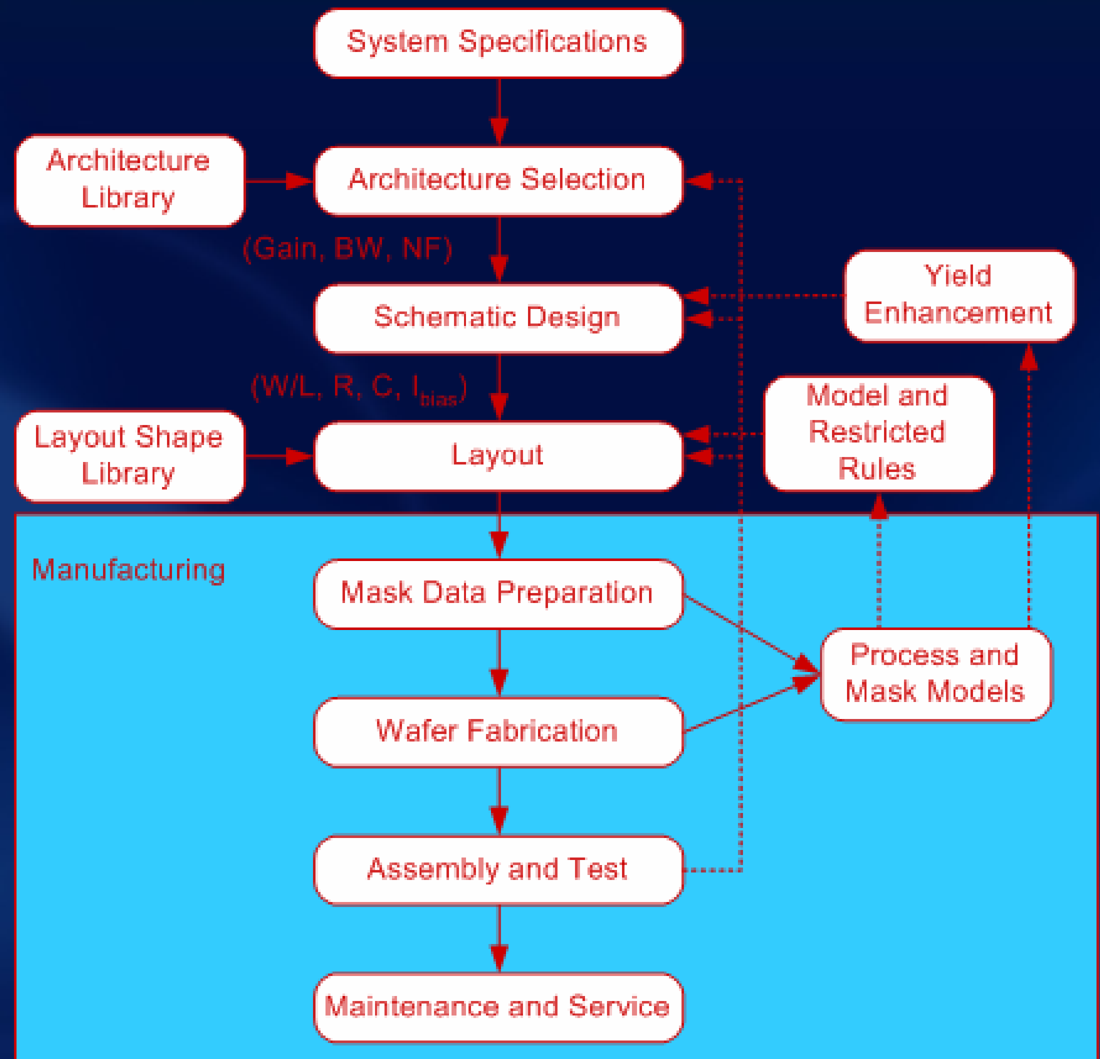
June 16, 2005

Contents

- Introduction
- Background
- Proposed Approach
- Implementation Issues
- Examples and Preliminary Results
- Discussions and Conclusions

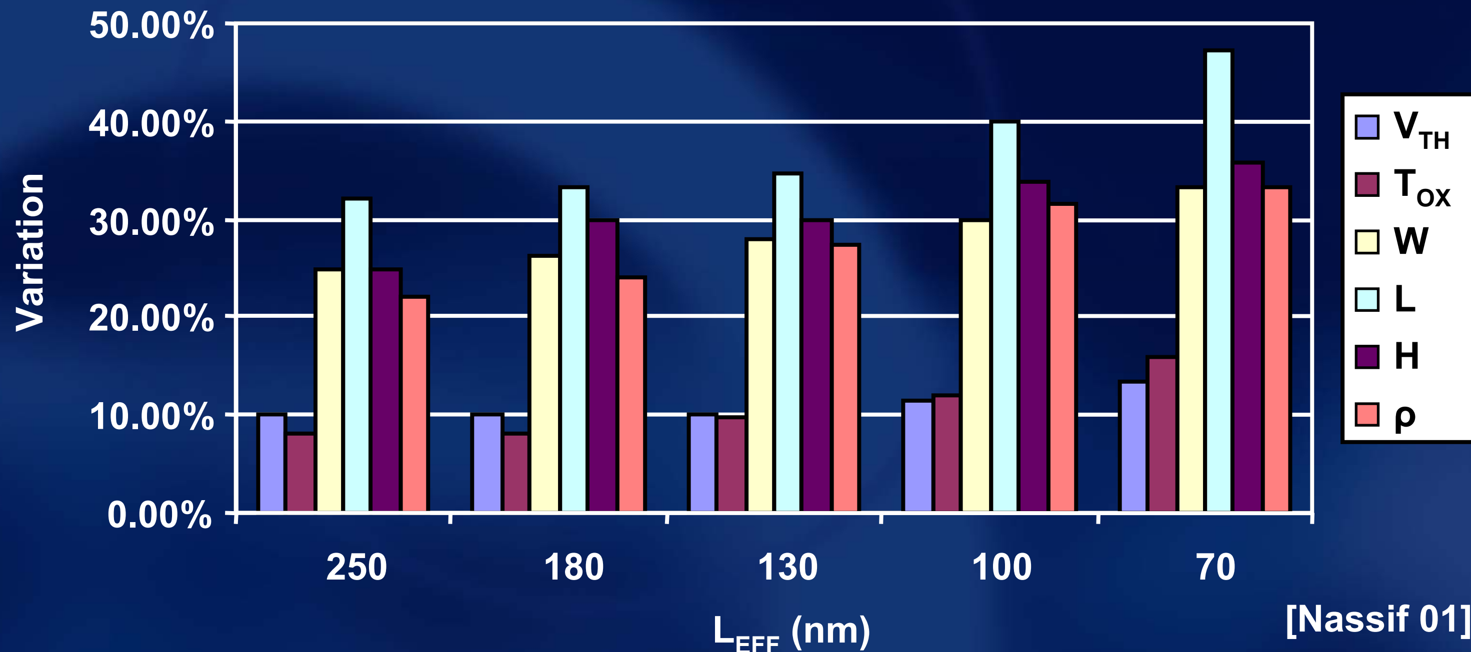
Introduction

- **Design-manufacturing interface is becoming more and more complex**
- **RF and analog integrated circuits are very sensitive to process variation**

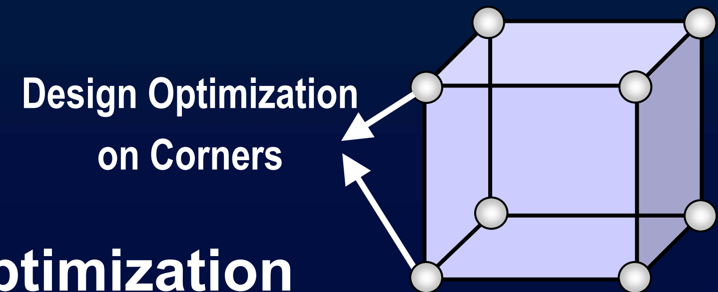


Trends of variability

- **Variability in DSM technologies is increasing**
- **Large-scale variation results in lower product yield**
- ***Control performance variability in early design stages***



Traditional Corner-Enumeration Optimization



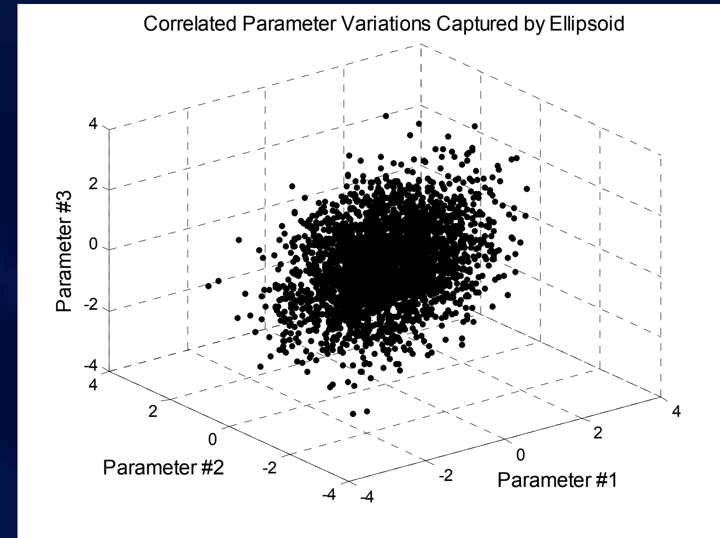
- Corner-enumeration worst-case optimization
  - Most widely used robust design technique
  - Uncertain parameters are often assumed to have independent uniform distributions
  - Design is optimized for all corners of a $\pm 3\sigma$ tolerance box
- Problems with corner-enumeration optimization
  - Often ignores correlation between process parameters
  - Problem size increases exponentially in number of uncertain parameters
  - No guarantee for parameter points inside the $\pm 3\sigma$ tolerance box
  - Design for all corners could result in over-design

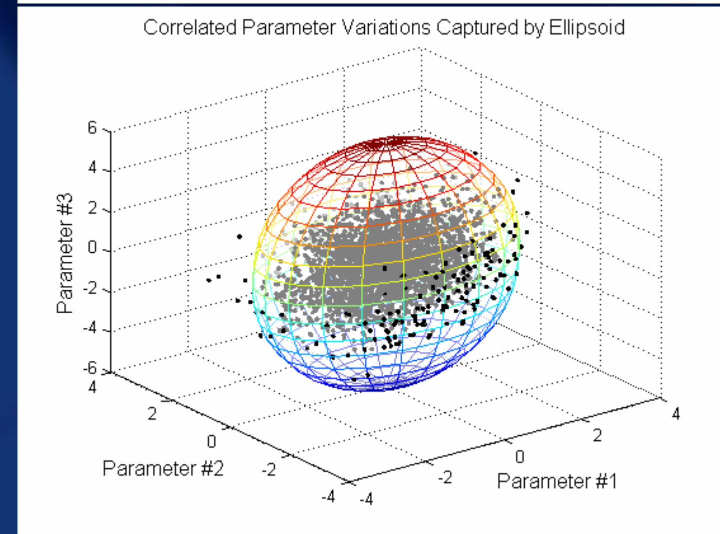
Contents

- Introduction
- Background
- Proposed Approach
  - Capturing process variations
  - Robust optimization approach
- Implementation Issues
- Examples and Preliminary Results
- Discussions and Conclusions

Sources and Statistics of Variability

- **Environment variations**
  - **Power supply voltage**
  - **Temperature**
  - **Noise coupling**
- **Model environmental variations by Uniform distributions and capture their variability by *polyhedron***
- **Manufacturing variations**
  - **Device**
  - **Interconnect**
- **Model manufacturing variations by Normal distributions and capture their variability by *ellipsoid***





Capturing the process variation

- **Process variation statistics are characterized by joint-pdf [Nassif'01]**
  - **Independent Gaussian random variables**
  - **Correlated Gaussian random variables**
- **Multivariate Gaussian Distribution (μ, Σ)**

$$p_X(X) = \frac{1}{(2\pi)^{n/2}|\Sigma|^{1/2}} \exp\left\{-\frac{1}{2}(X-\mu)^T \Sigma^{-1} (X-\mu)\right\}$$

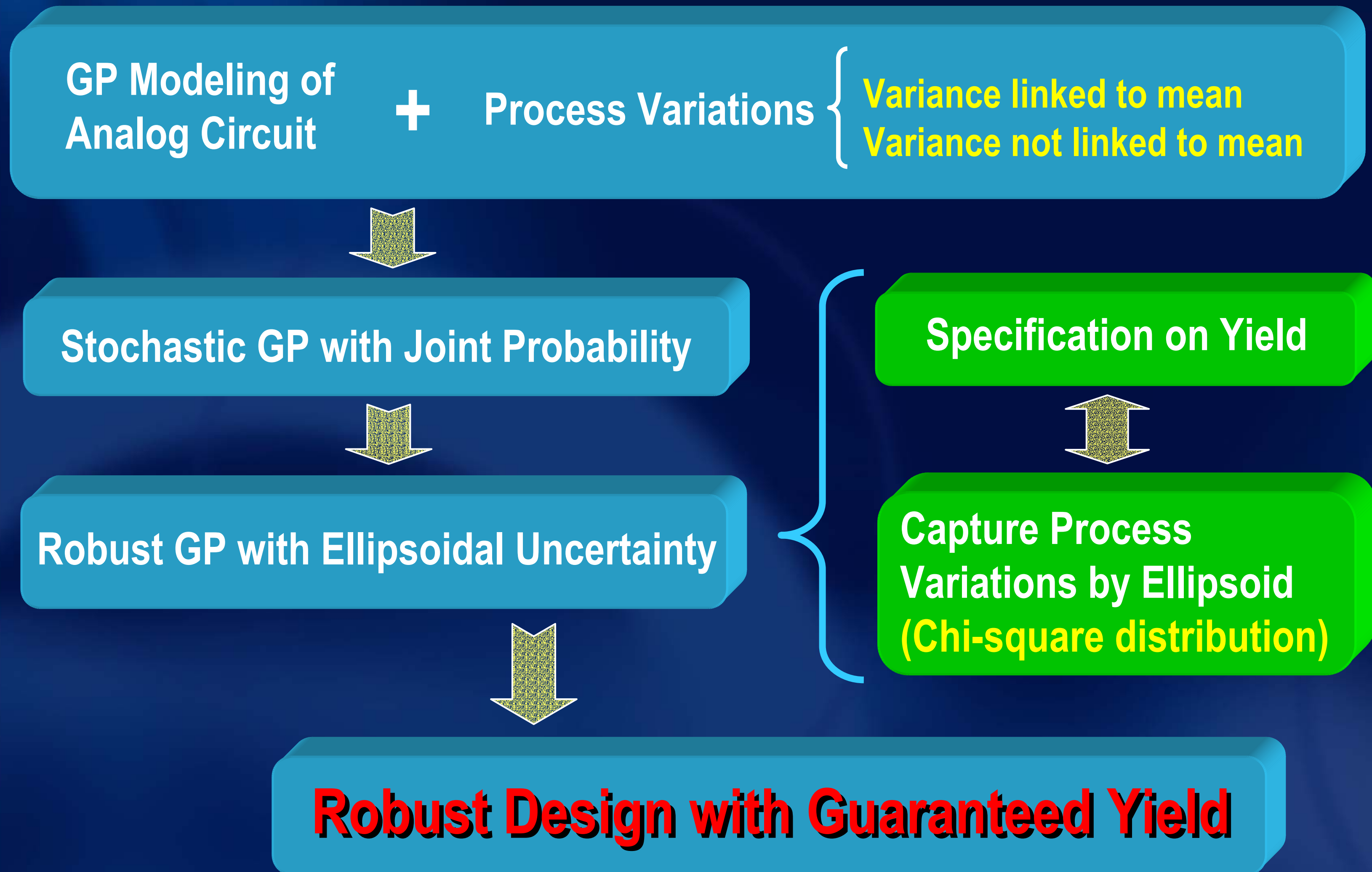
- **Equidensity contour is concentric ellipsoid**

$$U = f(\mu,\Sigma,r) = \left\{ X \in R^n \;\middle|\; (X-\mu)^T \Sigma^{-1} (X-\mu) \le r^2 \right\}$$

- **Probability has a chi-square distribution with degree *n***

$$\text{Prob}\left(u \in U\right) = F_{\chi_n^2}(r^2)$$

OPERA Concept



Robust Optimization Approach

- **Robust geometric programming†**
  - Robust GP incorporates a model of data uncertainty and optimizes for the worst-case scenario under the model
  - Computation time increases linearly in number of uncertain parameters
- **Design for variability via robust GP:**
  - Many analog IC design for variability problems can be cast as robust GPs
  - Handles correlated statistical variations in both process parameters and design variables
  - Can carry out robust designs with required yield bound
  - Results in less over-design (compared with corner-enumeration optimization)

† ***More details can be found in "Tractable Approximate Robust Geometric Programming", revised for publication, May 2005***

Contents

- Introduction
- Background
- Proposed Approach
- Implementation Issues
  - Variance-linked-to-mean uncertainty
  - Variance-not-linked-to-mean uncertainty
- Examples and Preliminary Results
- Discussions and Conclusions

Modeling Process Variations

- **Variance-linked-to-mean variation**
  - Relative variations (e.g. ΔR/R, ΔC/C),

  i.e. variance is proportional to mean
  - Model the variations in process parameters by

$$\delta p_i / p_i \sim N(0, \sigma_i^2), \; i = 1, \ldots, q$$

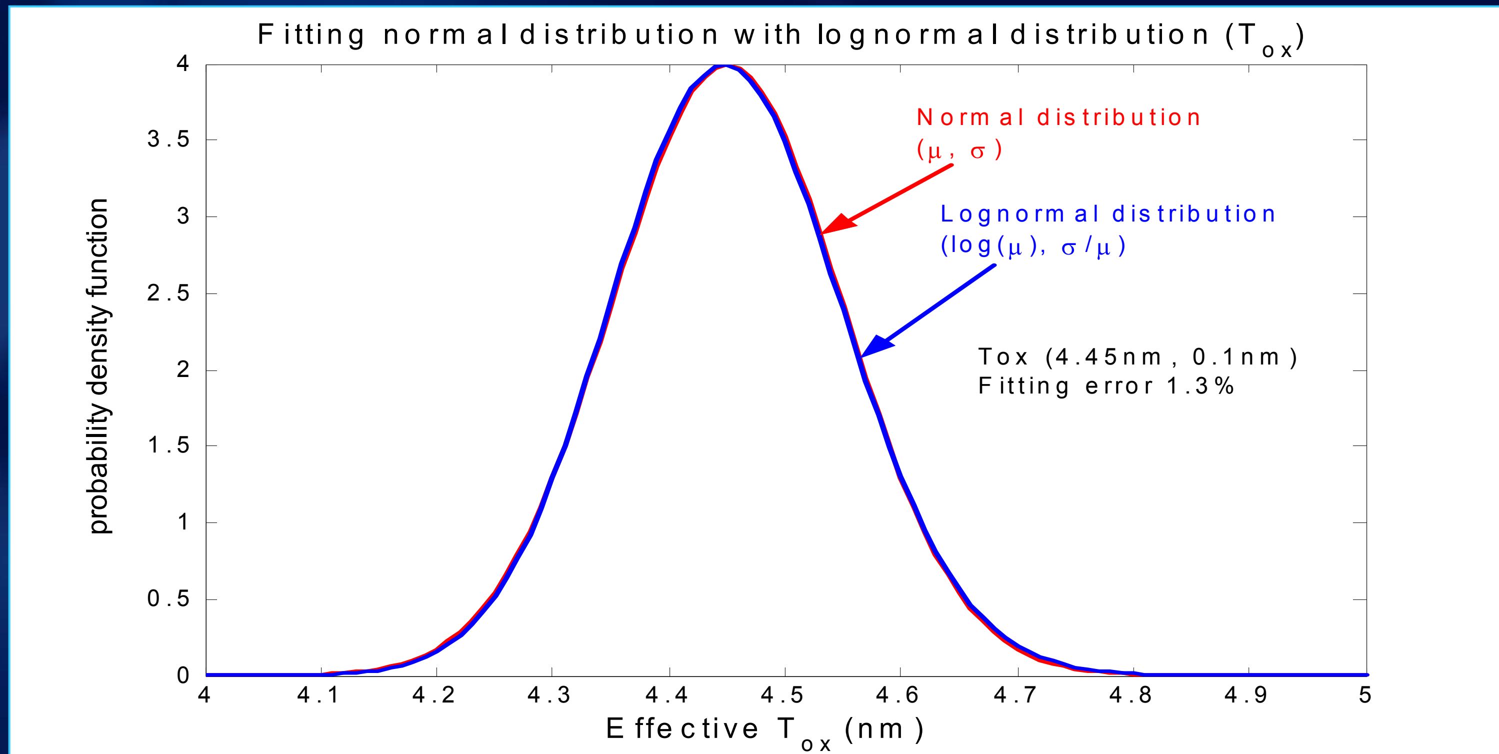
- **Variance-not-linked-to-mean variation**
  - Absolute variations (e.g. ΔW, ΔL, ΔV_{th}),

  i.e. variance is independent of mean
  - Model the variations in both design variables and process parameters as

$$\delta p_i \sim N(0, \sigma_{p_i}^2), \; i = 1, \ldots, q, \quad \delta x_j \sim N(0, \sigma_{x_j}^2), \; j = 1, \ldots, n$$

Lognormal approximation

- **Narrow normal distribution can be approximated as lognormal distribution**
  - **Most process parameter variation satisfy this condition (e.g. tox)**



μ=4.45nm, σ=0.1nm

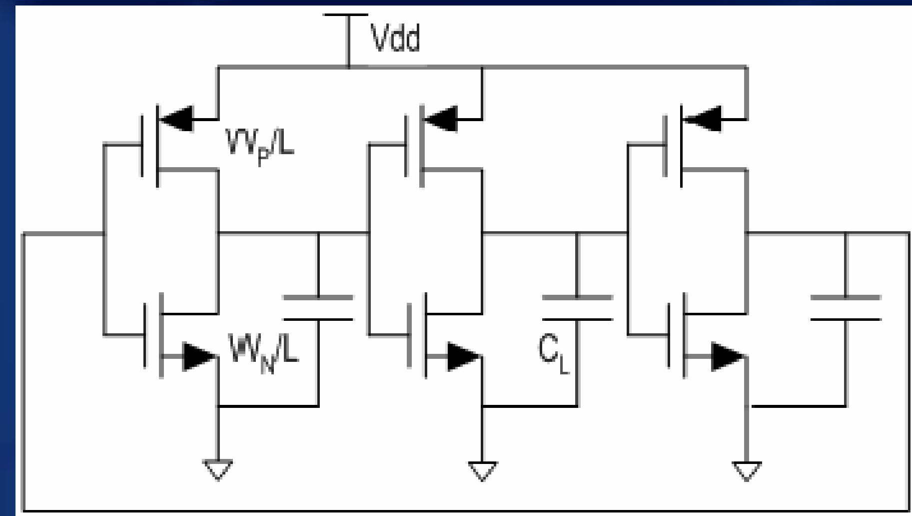
Contents

- Introduction
- Background
- Proposed Approach
- Implementation Issues
- Examples and Preliminary Results
  - Ring Oscillator Example
  - LC Voltage-Controlled Oscillator Example
- Discussions and Conclusions

Ring Oscillator Design Example

- **5GHz Ring Oscillator design example**
- **IBM 7HP 1.8V 0.18μm BiCMOS process**
- **Design Variables:**
  - **W_{eff}, L, ΔV**
- **Design objective and constraints:**

Minimize **Power**
Subject to **Phase Noise ≤ PN_max**
f _resonant = f_0



Robust Ring Oscillator Design Results

- Optimization results (90% yield bound for robust GP, Freq: 5±1 GHz):

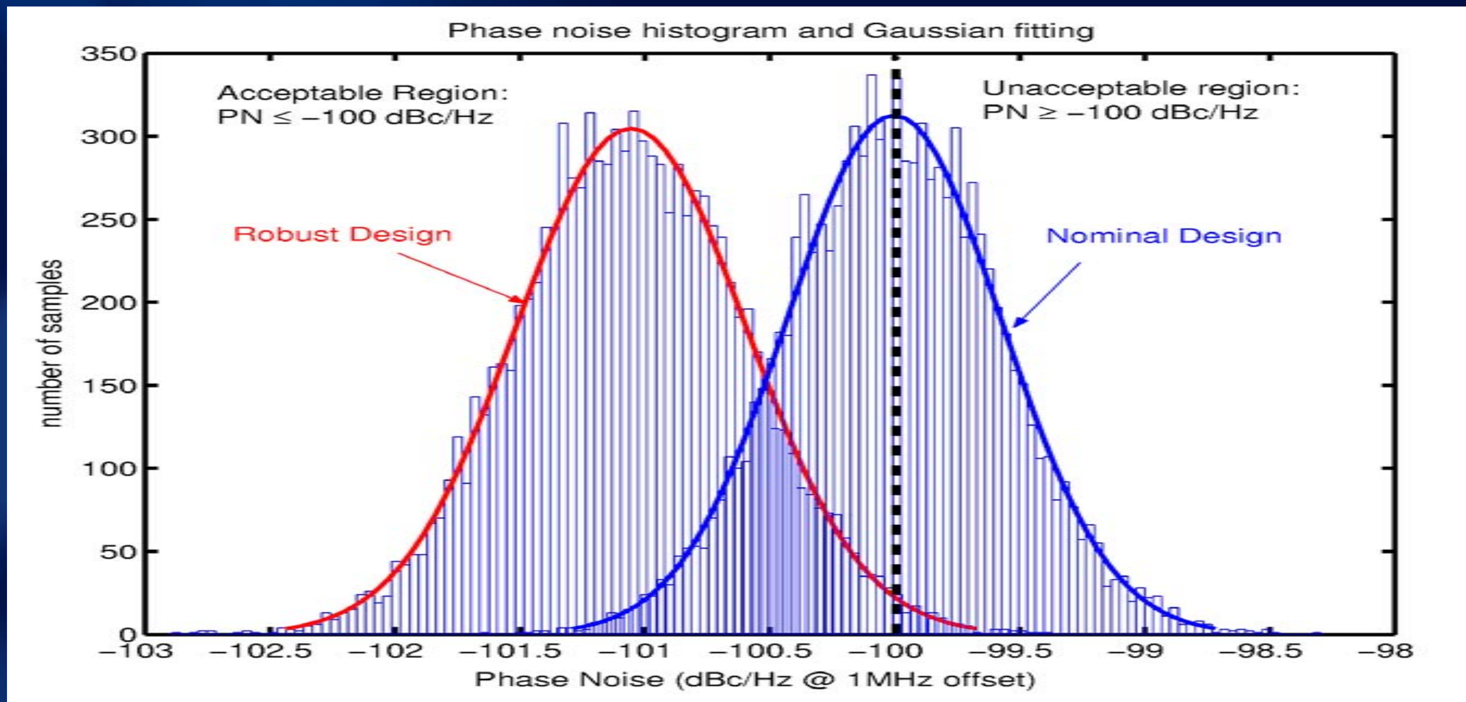
Design Variables	GP Design	Robust GP Design
Weff	4.53μm	6.68μm
Length	0.26μm	0.24μm
ΔV	0.42V	0.387V

Specifications	GP Design	Robust GP Design
Power	1.87mW	2.59mW
Yield	50%	**≥ 90%**
Phase Noise	-100dBc/Hz	-101dBc/Hz
Frequency	5GHz	4.85GHz

- Robust design achieve better yield with higher design cost

Monte Carlo Verification

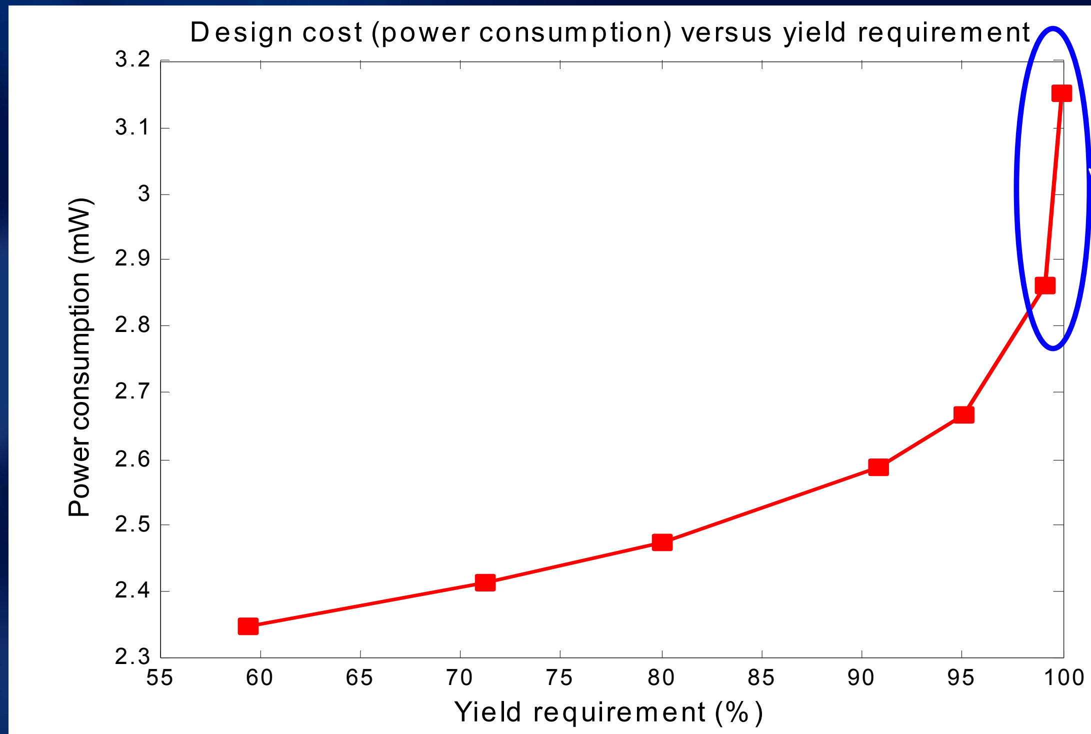
- **Actual yield is estimated by Monte Carlo analysis with 10K samples**



- **Optimization without considering process variation (i.e. nominal design) might have very low yield (50% in this example)**
- **Robust GP design achieved guaranteed yield ≥ 90%**

Design Cost vs. Yield Requirement

- **Trade-off curve of power consumption (design cost) versus yield requirement**

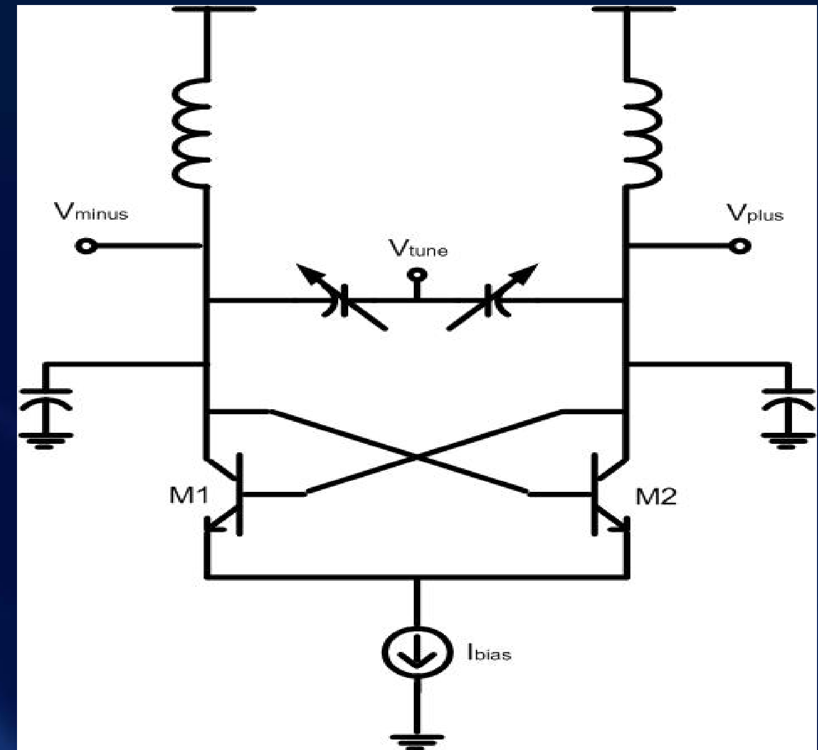


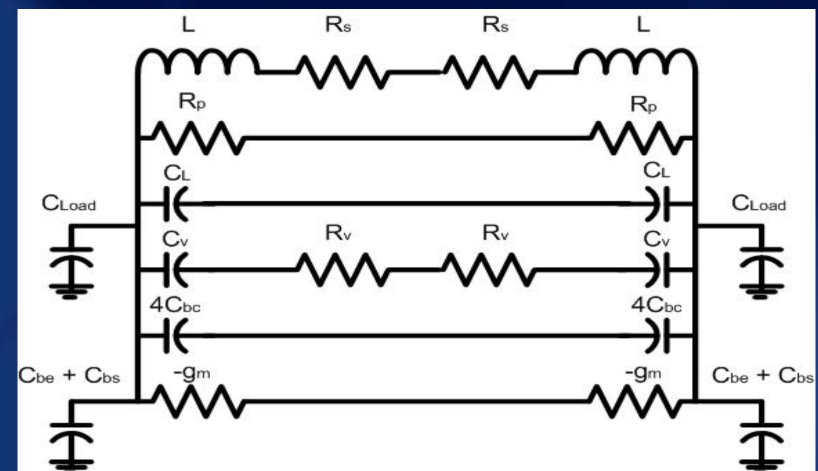
Very high design cost to achieve yield approaching 100%

- **Design cost increases when yield requirement increases**

Voltage-Controlled Oscillator Design Example

- **2.1GHz LC VCO design example**
- **Hitachi SiGe BiCMOS process using 90GHz f_T NPN**
- **Differential VCO is equivalent to a tank model**





VCO Experiment Setup

- **Design Variables:**
  - I_bias, g_tank, C_tank, L, Vsw
- **Design objective and constraints:**

Minimize	Power
Subject to	Phase Noise ≤ PN_max
	Loop Gain ≥ LG_min
	L_tank*C_tank*ω^2 = 1
	Vsw ≤ Vdd
	Vsw ≤ I_bias/g_tank

- **Design Uncertainty:**

$$\left(\frac{\Delta C_{\text{tank}}}{C_{\text{tank}}}, \frac{\Delta g_{\text{tank}}}{g_{\text{tank}}}, \frac{\Delta L}{L}\right) \sim N(0, \begin{Bmatrix} \sigma_1^2 & \sigma_{12}^2 & \sigma_{13}^2 \\ \sigma_{21}^2 & \sigma_2^2 & \sigma_{23}^2 \\ \sigma_{31}^2 & \sigma_{32}^2 & \sigma_3^2 \end{Bmatrix})$$

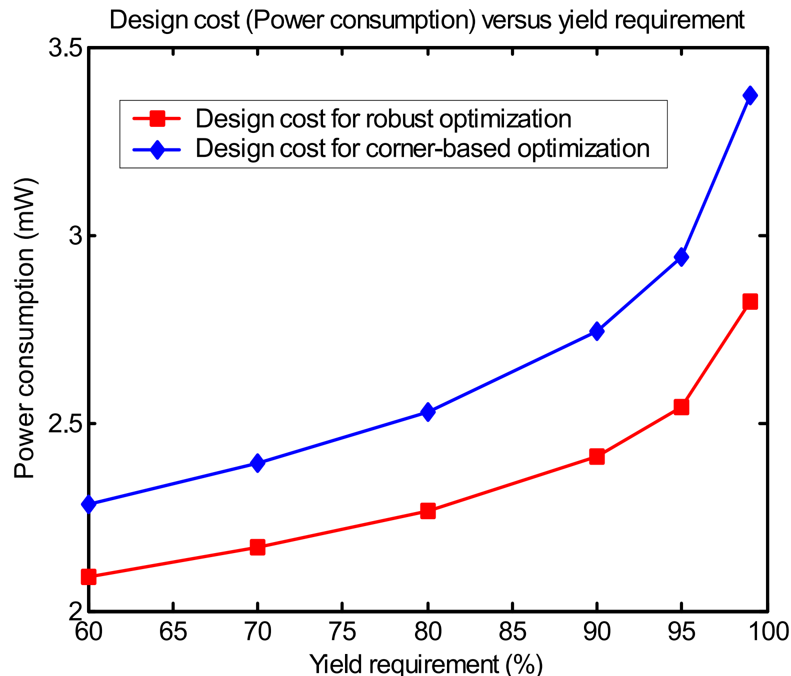
VCO optimization results

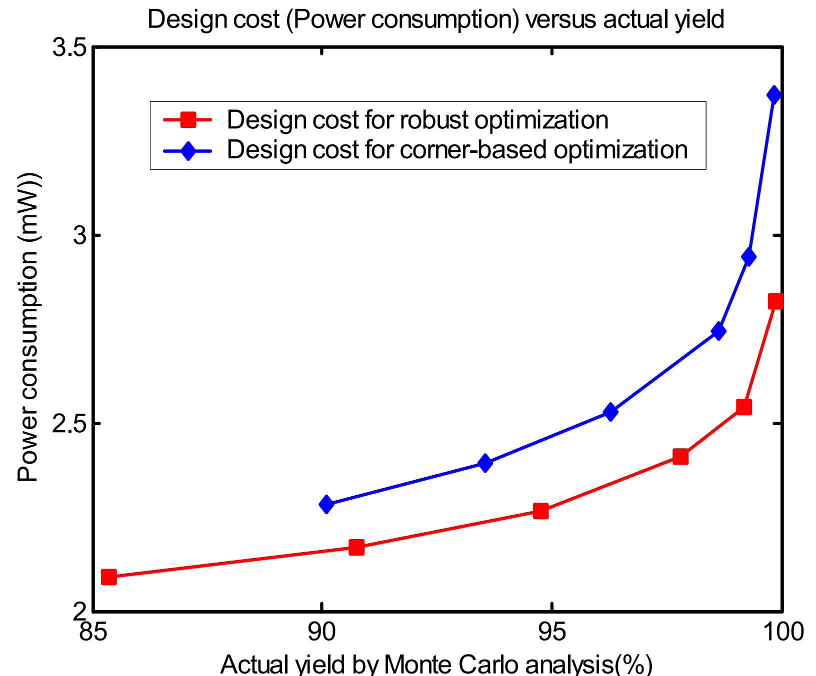
- **Robust GP yield bound:**
  - **Yield bound can be set by adjusting the ellipsoid radius**
- **Corner selection — vertices of polyhedron**
  - **Confidence ellipsoid in the robust optimization is inscribed in this polyhedron**
- **Optimization results (for 90% yield bound, Freq: 2.1±0.4GHz)**

	Robust optimization	Corner - enumeration optimization
I_bias	2.41mA	2.72mA
C_tank	1.33pF	1.26pF
g_tank	0.894mS	1.018mS
L	2.83nH	2.82nH
Vsw	2.5V	2.5V

LC Oscillator design cost vs. yield bound and actual yield

- Yield is estimated by 10K Monte Carlo analysis
- Design cost increase when yield requirement increase
- 20% over design for $\pm 3\sigma$ actual yield in corner-based optimization compared to robust optimization





Contents

- Introduction
- Background
- Proposed Approach
- Implementation Issues
- Examples and Preliminary Results
- Discussions and Conclusions

Discussions and Conclusions

- Ellipsoidal uncertainty captures both independent and correlated process variations
- Yield requirement can be explicitly incorporated as a design constraint
- Robust optimization using posynomial equations (requires fewer simulations)
- Guaranteed yield bound by assuring all parameters within the ellipsoid instead of sampling the process variation
- Handles both parameter and design variable uncertainty
- Achieve the same yield with much less over-design (compared with corner-enumeration optimization)