ORACLE
Optimization with Recourse of Analog Circuits including Layout Extraction

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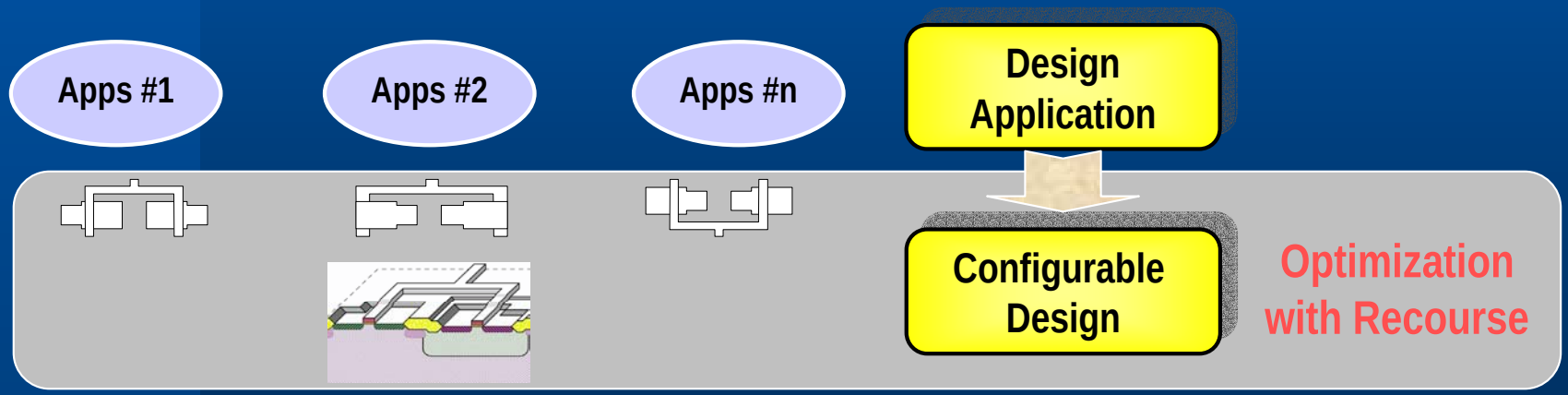
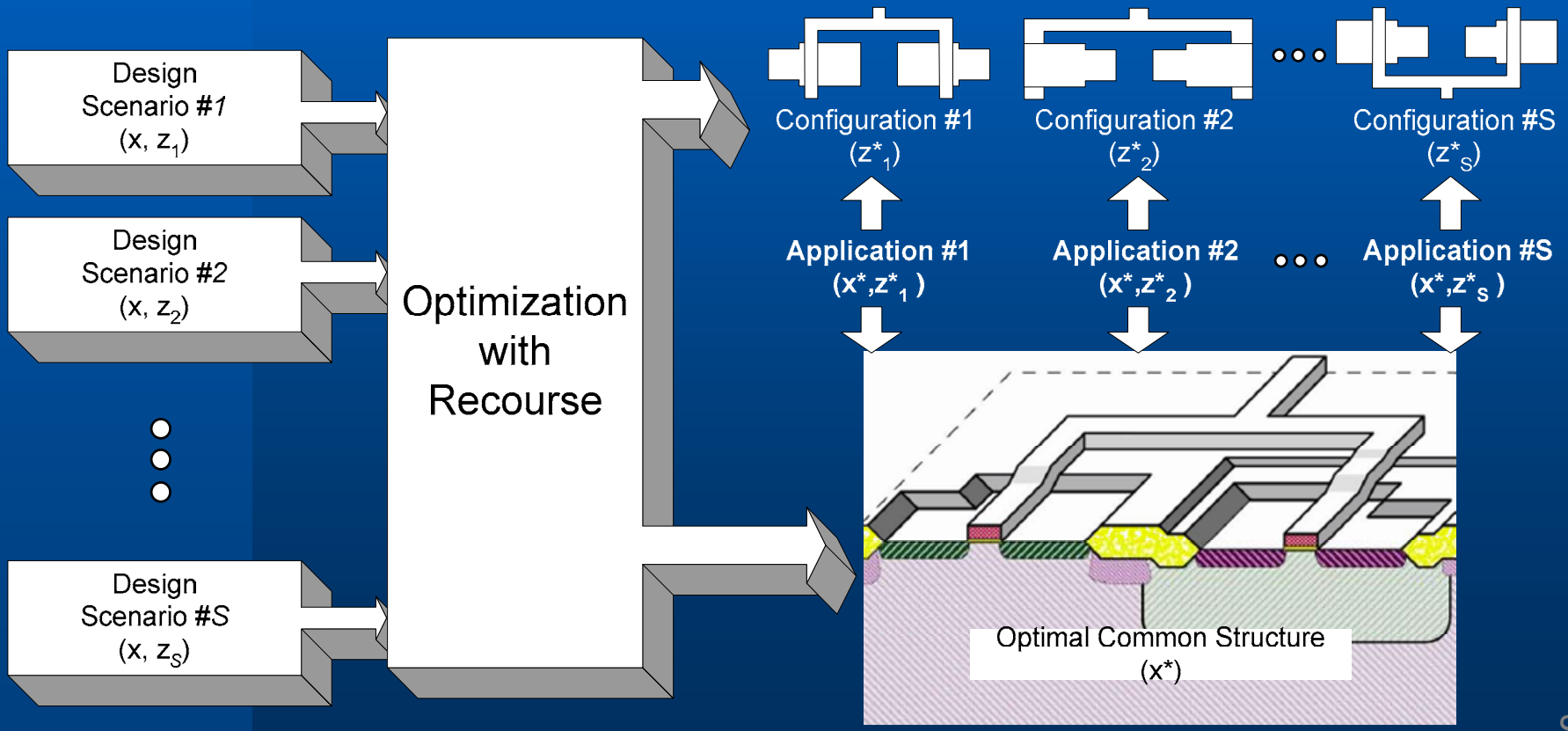
Analog/RF IC Cost Crisis

- Analog design risk makes application-specific costs unaffordable for many applications
  - Difficult to predict silicon realities w/o multiple silicon spins
- Regularity and reuse required for predictability and cost
- ORACLE: new optimization framework for creation of an application-domain-specific design fabric



ORACLE Methodology

- **Optimization for configurable analog/RF circuits**
  - **Initial focus is on BEOL mask configurable fabrics**
  - **Note that configurations are not limited to original scenarios**



Two-stage design process

- **Divide circuit design process into 2 stages**
  1. Optimize for representative set of applications based on chosen circuit topology and shared design variables
  2. Given common design fabric based on shared variables, optimally map a circuit design for a specific application
- **Methodology relies on efficient optimization formulation**
  - Stage 1 requires exploring large design space for many design scenarios
  - Importantly, modeling accuracy is not critical for stage 1 to define fabric
  - Detailed models and characterizations req'd for stage 2

Geometric Program with Recourse (GPR)

- **GPR formulation is perfect approach for stage 1:**

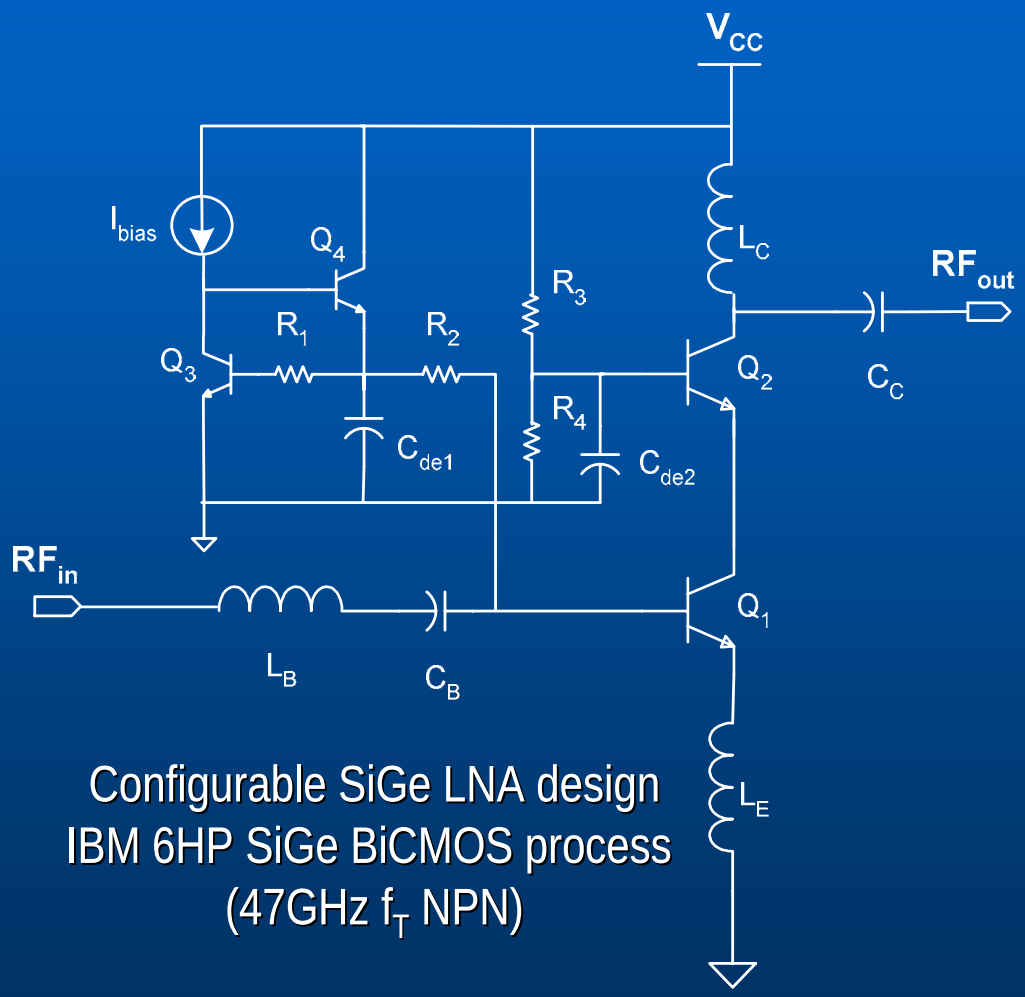
$$\begin{aligned} \text{minimize} \quad & F_0(x, z_1, \ldots z_S) \\ \text{subject to} \quad & F_i(x, z_i) \le 1, \quad i = 1, \ldots, m, \\ & G_i(x, z_i) = 1, \quad i = 1, \ldots, p, \\ & x_i > 0, \quad i = 1, \ldots, n, \\ & z_i > 0, \quad i = 1, \ldots, q. \end{aligned}$$

Where $F_i(x,z)$ are posynomial and $G_i(x,z)$ are monomial

- **GPR complexity grows linearly with number of scenarios**
- **Each individual design (scenario) is formulated and solved as a GP problem**

SiGe Low Noise Amplifier Example

- Selection of circuit topology and shared design variables is key
- Shared variables:
  - **Emitter length and width**
  - **Inductor outer dimension**
  - **Biasing BJT multipliers**
  - **Biasing Resistors**
  - **Decoupling caps**
- Application-specific variables:
  - **BJT multiplier**
  - **Inductor turns**
  - **Bias current and tuning caps**

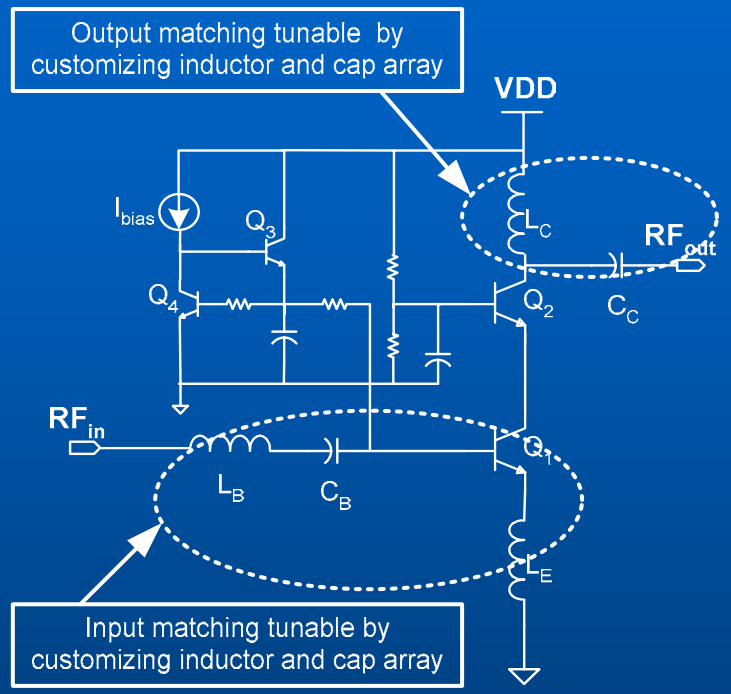


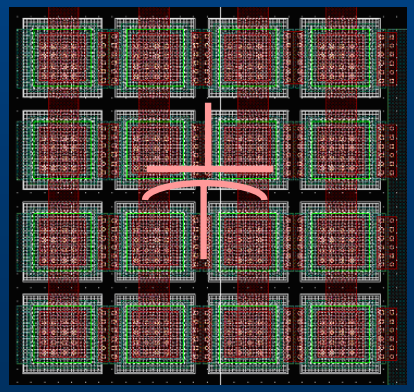
Configurable SiGe LNA design
IBM 6HP SiGe BiCMOS process
(47GHz f_T NPN)

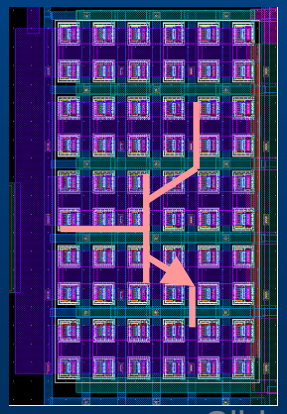
Frequency scalable LNA topology

- **Individual GP formulations for each scenarios:**
  - **12 design variables**
  - **28 inequality constraints**
  - **Solved using MOSEK™ MATLAB toolbox**
- **Input and output center frequency tunable**
- **SiGe BJT minimal NF is frequency scalable:**

$$NF_{min} \propto f, \text{ when } f << f_T$$

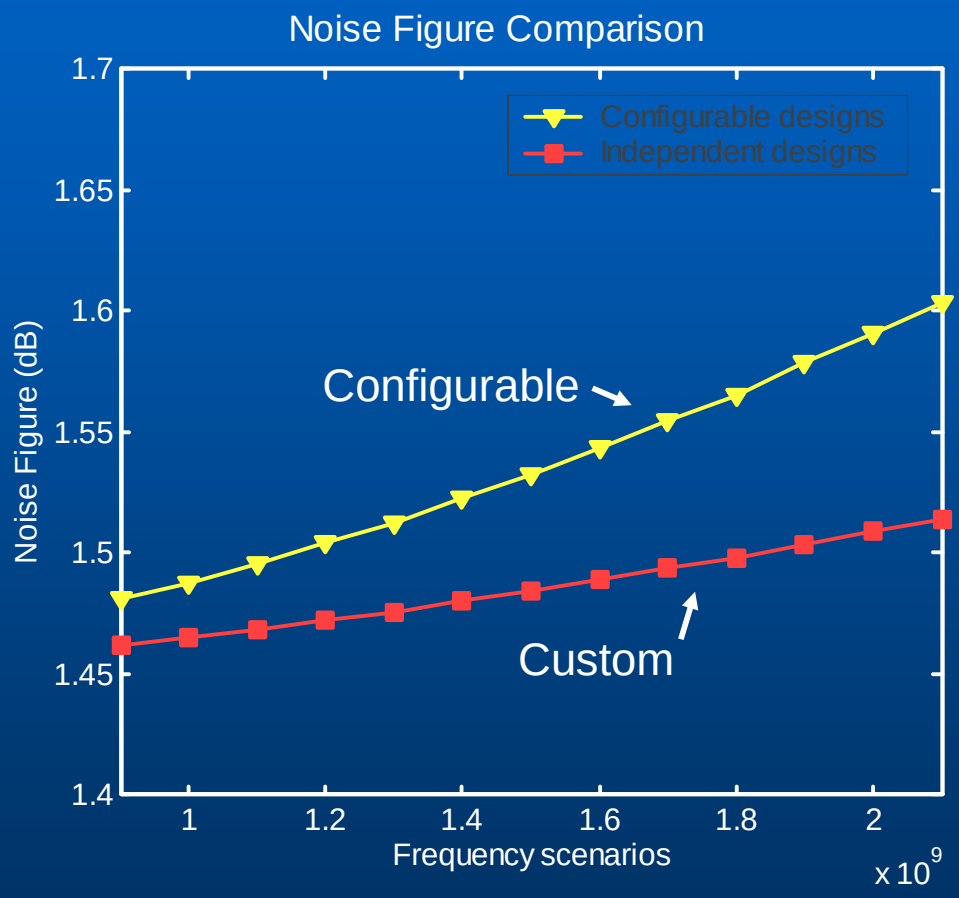






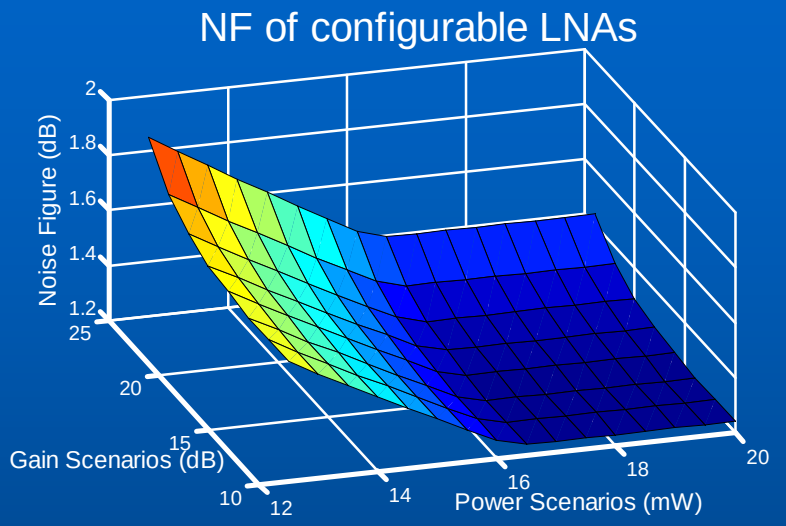
Center frequency configurable LNAs

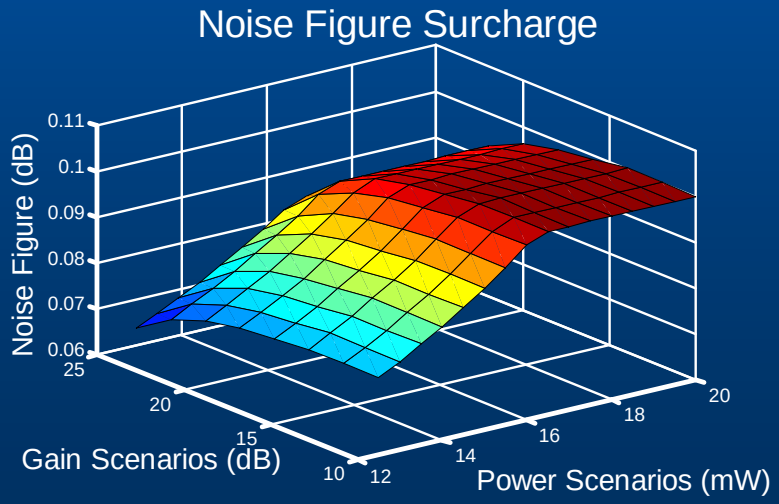
- **Consider center frequencies from 900MHz to 2.1GHz**
  - **13 design scenarios (200Mhz increments)**
  - **5+7×13 = 96 design variables**
  - **28 ×13 = 364 design constraints**
  - **Objective: Noise Figure**
- **13 custom designs produced as benchmark**
- **Performance comparable to custom designs with sufficient margin**



Power and gain configurable example

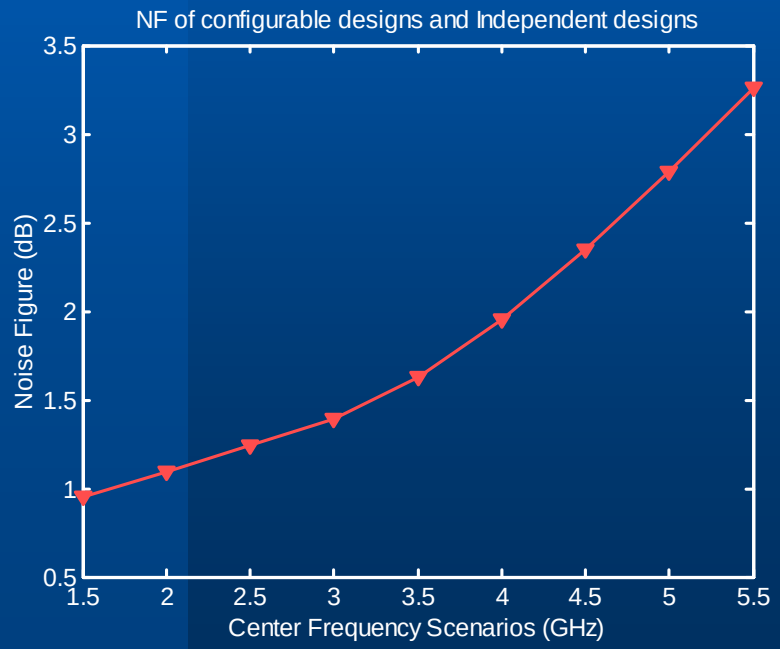
- 128 design scenarios by varying power and gain specifications
  - Power spec: 12.5→20mW by 0.5mW
  - Gain spec: 10→24dB by 2dB
- Resulting GPR problem
  - **8×16=128 design scenarios**
  - **5+7×128 = 901 design variables**
  - **28 ×128 = 3584 design constraints**
  - **Objective: Noise Figure**
- 128 custom designs produced as benchmark
- Efficiency
  - **1.5sec for 128 configurable design in 1.4GHz P4 machine**

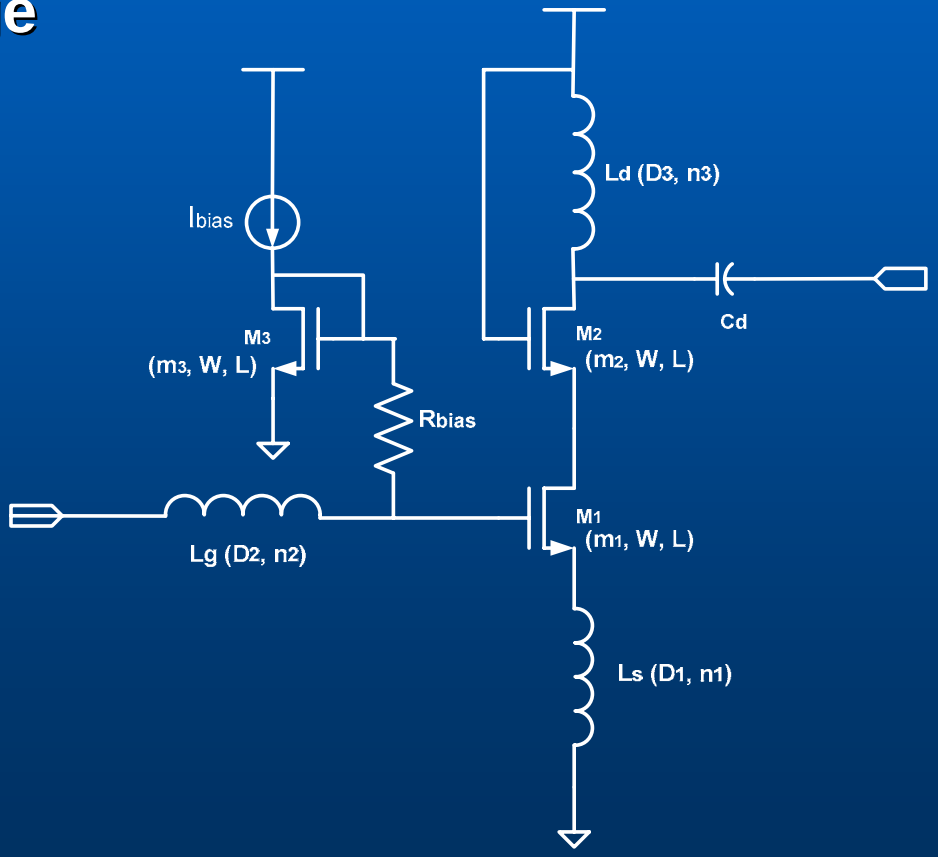




Configurable CMOS LNA example

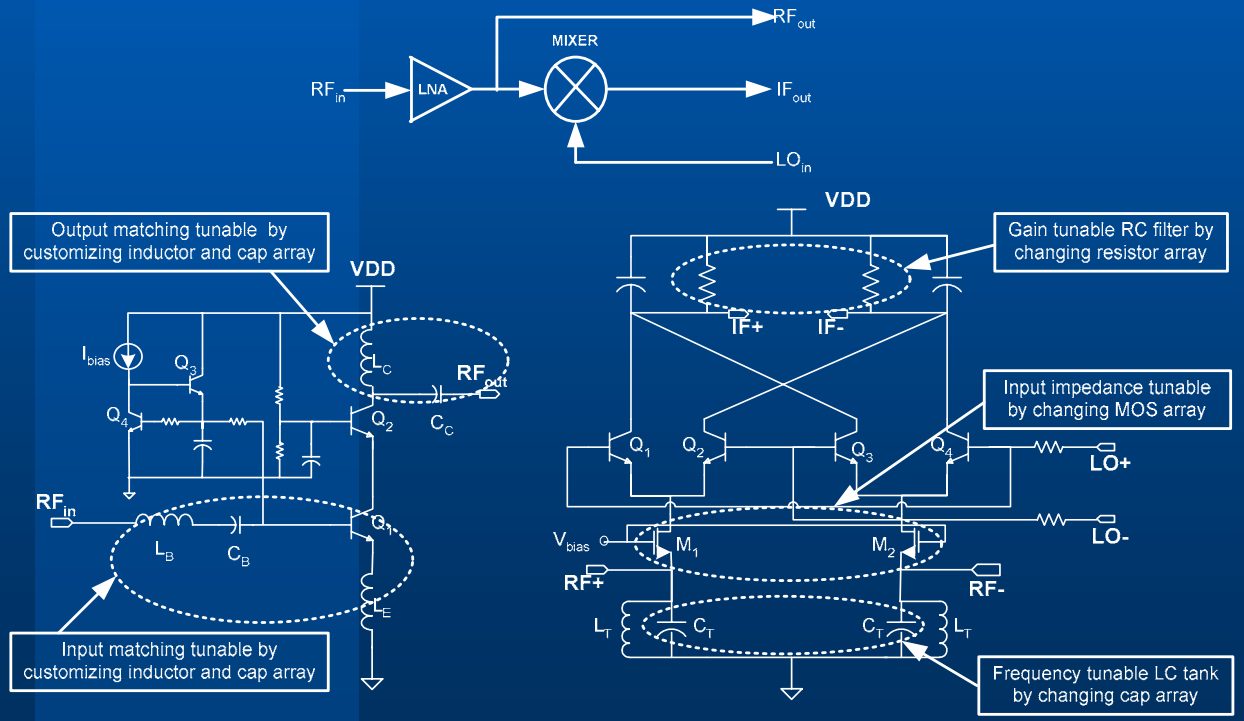
- **Vary center frequency from 1.5→5.5GHz by 500MHz**
  - 9 design scenarios
- **Objective: NF design surcharge**
- **NF's comparable to custom designs**

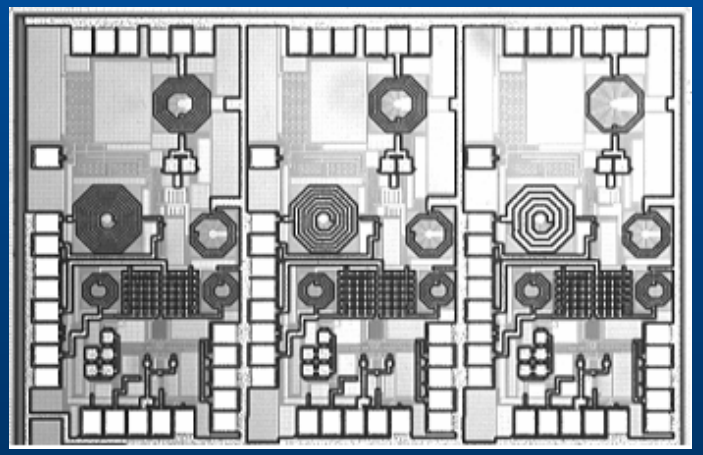




Configurable RF front-end silicon validation

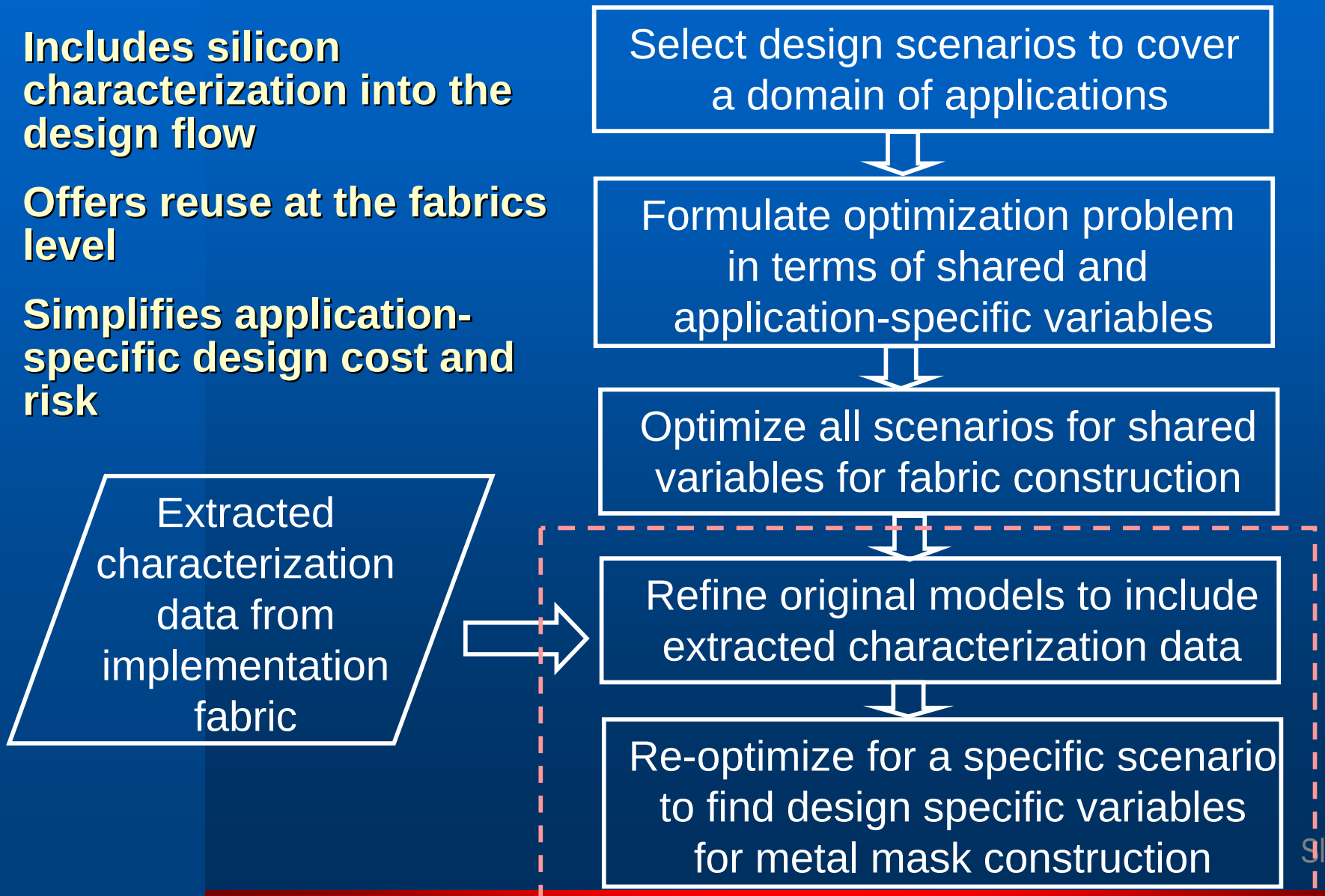
- 0.25μm 1P6M SiGe BiCMOS process (47GHz f_T NPN BJT)
- Targeted for 1.5GHz GPS, 2.1GHz WCDMA and 5GHz 802.11a applications
- Mapped to fabric via detailed simulation and extraction models





Regular Analog/RF IC Design Flow

- **Includes silicon characterization into the design flow**
- **Offers reuse at the fabrics level**
- **Simplifies application-specific design cost and risk**



Conclusions

- Configurable analog/RF circuits are required for many applications
  - Reduce design risk and manufacturing cost
- ORACLE proposed for optimization framework
  - Initial focus on mask configurable RF front-end circuits
  - Examples demonstrate promising possibilities
- Extending ORACLE to perform design centering to improve yield