Optimization of Phase-Locked Loop Circuits via Geometric Programming

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***Abstract*— We describe the global optimization of phase-locked loop (PLL) circuits using geometric programming (GP). Equations for the jitter, frequency range, and power of the PLL are presented in GP form. An array of PLL circuits was automatically generated using this technique in a $0.18\ \mu\mathrm{m}$, $1.8\mathrm{V}$ CMOS process. Silicon measurements show good agreement with the model. The results include a $1.9\mathrm{GHz}$ PLL with a period jitter of $2.2\mathrm{ps}$ RMS and an accumulated jitter of $6.2\mathrm{ps}$ RMS, consuming $10.8\mathrm{mW}$.**

I. Introduction

Phase-locked loops are an important building block of almost any synchronous digital system including communications, video, microprocessor, and many other applications. Each of these systems has vastly different frequency, jitter, power, and area requirements. In order to meet the various requirements, companies have focused on design reuse, creating a small library of individual phase-locked loop (PLL) designs with wide input and output frequency ranges. Until recently, the inherent design trade-offs with this approach were unknown. Fig. 1 shows how the power and accumulated jitter would trade-off with frequency range for a typical $2\mathrm{GHz}$ PLL in a $0.13\mu\mathrm{m}$ CMOS process. Each point on these trade-off curves represents a different PLL design, minimizing power and jitter respectively. As can be seen, an order of magnitude reduction in both specifications can be won by relaxing the VCO frequency range. The variations in the magnitude and slope of the curves are valuable pieces of information to the system level designer. Automating the PLL design to quickly obtain this information and to tailor the PLL design for the various applications is clearly advantageous.

This work describes a new method for the automation of PLL design via geometric programming (GP). This work is based on an approach that poses the analog circuit design problem as a special type of convex optimization problem [1]. Once the specifications are described in an equation form consistent with GP, optimal PLL designs over process, voltage, and temperature (PVT) variations including routed GDSII can be automatically generated. Section II gives a brief formulation of the geometric program. Section III introduces some simple GP transistor models. Section IV shows how to cast some key PLL specifications in GP form, with simulation results for comparison. Section V compares the optimization results with silicon measurements.

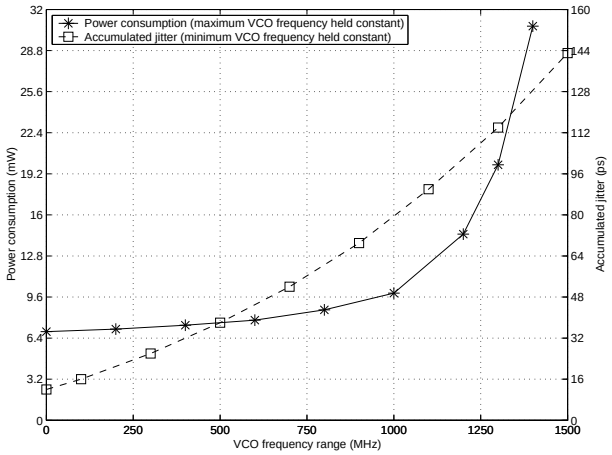

Fig. 1. PLL trade-off curves of power consumption and accumulated jitter versus VCO frequency range. Each point represents an optimal PLL design. For the power consumption trade-off curve, the maximum VCO frequency is constant while the minimum VCO frequency is swept. For the accumulated jitter trade-off curve, the minimum VCO frequency is constant while the maximum VCO frequency is swept.

II. Geometric programming

Let g be a real-valued function of n real, positive variables $x_1, x_2, \ldots, x_\mathrm{n}$. A monomial function, g, has the form

$$g(x_1, \ldots, x_n) = c x_1^{\alpha_1} x_2^{\alpha_2} \cdots x_n^{\alpha_n}$$

where $c \geq 0$ and α_i is a real number. A posynomial function is a sum of monomials.

A geometric program [2] has the form

$$\begin{array}{ll} \text{minimize} & f_0(x) \\ \text{subject to} & f_i(x) \leq 1, \quad i = 1, 2, \ldots, m, \\ & g_i(x) = 1, \quad i = 1, 2, \ldots, p, \\ & x_i > 0, \quad i = 1, 2, \ldots, n, \end{array} \tag{1}$$

where f_i are posynomial functions and g_i are monomial functions. If the circuit design problem can be cast in this format, it can be reformulated as a convex optimization problem [3]. Newly developed interior-point method algorithms can be used to solve this problem efficiently. The result is either a globally optimal solution, or a proof that the design is infeasible (*i.e.* the specifications are too tight).

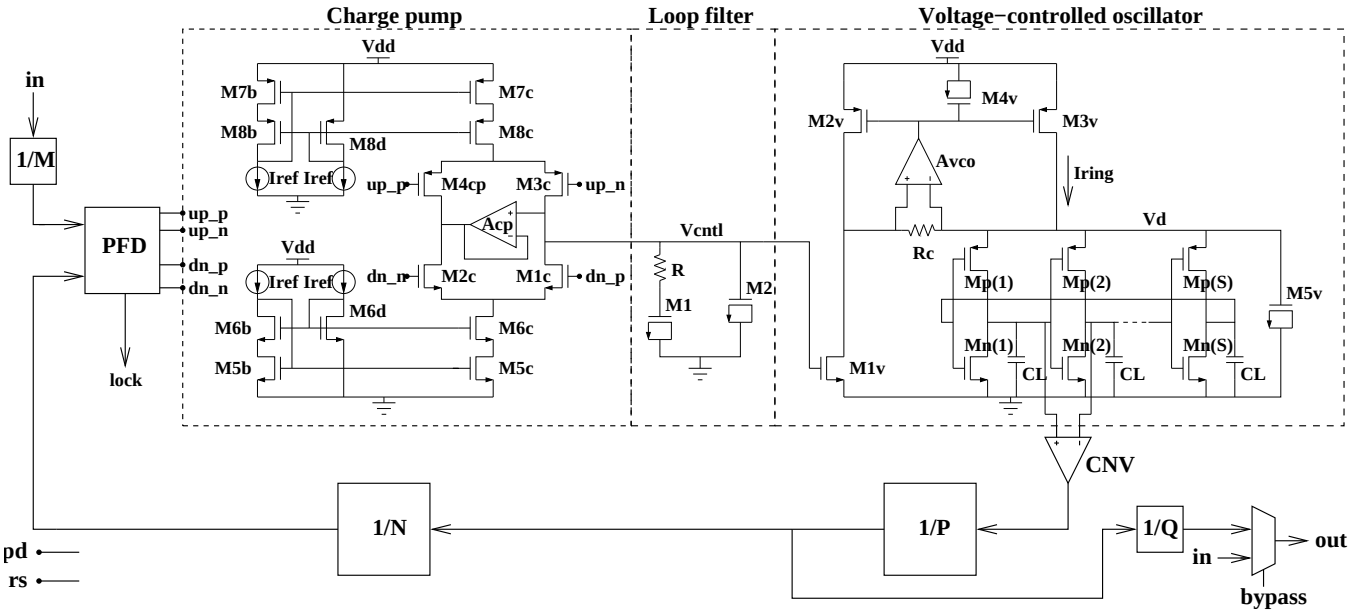

Fig. 2. Block diagram of the PLL showing charge pump, loop filter, and VCO subcircuits. The optimization variables include the lengths and widths of all devices, as well as the number of stages in the ring oscillator. The output of the optimization is a sized, routed layout (in GDSII format).

III. GP compatible transistor models

Long-channel, saturation region models for a MOS transistor's gate overdrive voltage ($V_{\rm gov} = V_{\rm gs} - V_{\rm t}$), transconductance ($g_{\rm m}$), and gate-source capacitance ($C_{\rm gs}$) are shown in (2).

$$\begin{array}{lll} V_{gov} & = \sqrt{\frac{2I_dL}{\mu C_{ox}W}} & = \sqrt{\frac{2}{\mu C_{ox}}}W^{-0.5}L^{0.5}I_d^{0.5} \\ g_m & = \sqrt{2\mu C_{ox}\frac{W}{L}I_d} & = \sqrt{2\mu C_{ox}}W^{0.5}L^{-0.5}I_d^{0.5} \\ C_{gs} & = \frac{2}{3}C_{ox}WL & = \frac{2}{3}C_{ox}W^{1.0}L^{1.0}I_d^0 \end{array} \quad (2)$$

It can be seen that $V_{\rm gov}$, $g_{\rm m}$, and $C_{\rm gs}$ are monomial functions of the process constants and design variables (W, L, and $I_{\rm d}$). GP compatible models can be generated for all large and small signal characteristics of the transistor. Similar, but more complex, GP models are utilized in the PLL optimization problem which take into account finite output impedance, body effect, short-channel effects, and other non-idealities.

IV. Clock generation PLL design in GP form

A simplified version of the clock generation PLL topology chosen for optimization is shown in Fig. 2. The charge pump based PLL with integrated loop filter and single-ended ring oscillator is well documented in the literature [4], [5]. An active cascode in the VCO with optimized decoupling capacitors ensures superior low and high frequency PSRR performance. Low power dividers, fixed or up to 12-bit programmable, can be chosen for input, output and feedback dividers. This proven PLL topology has a good power/jitter trade-off and a wide range of operating frequencies, making it an excellent target for optimization.

The optimization variables include the lengths and widths (L, W) of all transistors and resistors, as well as the number of stages in the ring oscillator (S). The specifications and possible optimization objectives include area, power, accumulated jitter, static phase error, phase margin, input and output frequencies, jitter due to power supply noise, and so on. The GP formulation of a few of these key specifications follows.

The first step in formulating the PLL optimization problem involves describing the process and topology constraints in GP form. Some examples are presented here. A variety of posynomial inequalities, such as lithographic constraints (*e.g.* $L_{\rm M1} \geq L_{\rm min}$), defines the design space of the optimization variables. Monomial equalities are used to set current relationships, such as $I_{\rm d,M5c} = I_{\rm d,M7c}$ and $I_{\rm ring} = I_{\rm d,M3v}$. Equalities such as $V_{\rm gov,M2v} = V_{\rm gov,M3v}$ and $L_{\rm M2v} = L_{\rm M3v}$ set up proper biasing conditions for current mirrors. Constraints are added for good design practice, such as $L_{\rm M2v} = L_{\rm M4v}$, to reduce threshold voltage mismatch; and $L_{\rm M5v} \leq 1\mu$m, to reduce channel resistance. The $\frac{1}{f}$ noise upconversion into the oscillator's phase noise spectrum is minimized by setting $L_{\rm Mn} = L_{\rm Mp}$ and by proper sizing of the ratio, r, where $W_{\rm Mp} = rW_{\rm Mn}$ [6]. Very little error is introduced in setting up the process and topology constraints. As an example, Fig. 3 compares the GP prediction for $V_{\rm gs,M5b}$ with extracted simulation results over multiple designs and worst-case PVT variations in a 0.13μm process.

A. Power consumption

Power consumption can be expressed in posynomial form:

$$\begin{array}{ll} Power & = V_{dd}\left(4I_{ref} + I_{d,M5c} + I_{d,M2v} + I_{d,M3v}\right) \\ & +power_{Acp} + power_{Avco} + power_{digital}. \end{array} \quad (3)$$

The $power_{\rm digital}$ includes the power consumption for the PFD, small-swing to CMOS converter (CNV), buffers, as well as the power of all dividers. The power consumption for each of the operational amplifiers, $A_{\rm cp}$ and $A_{\rm vco}$, is a posynomial

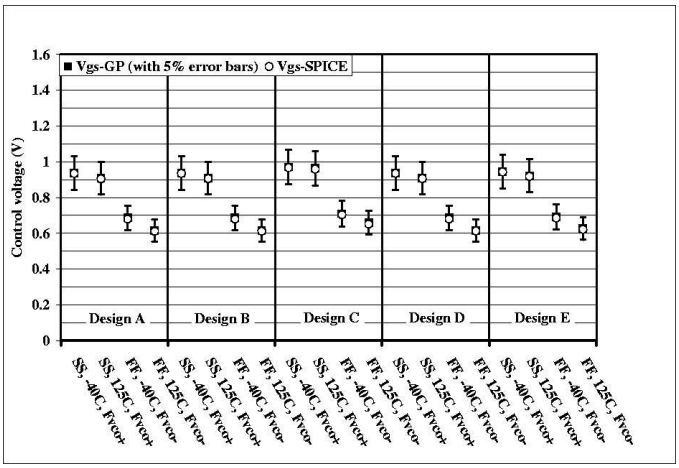

Fig. 3. Bias voltage of charge pump, $V_{\mathrm{gs,M5b}}$, comparing GP optimization results versus extracted SPICE simulation results over multiple PLL designs and worst-case PVT variations.

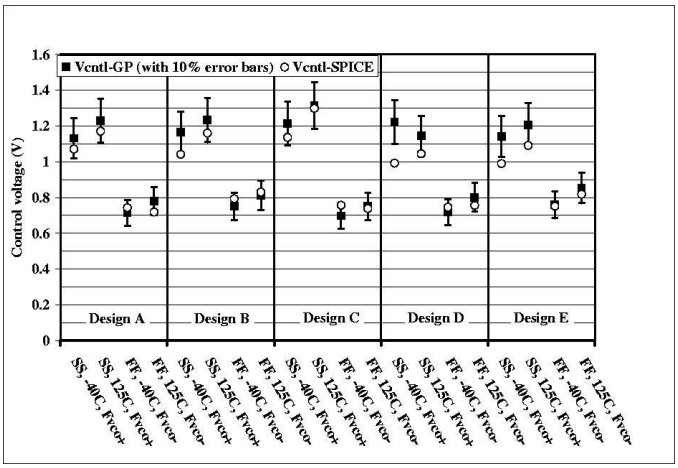

Fig. 4. Control voltage, V_{cntl}, of PLL comparing GP optimization results versus extracted SPICE simulation results over multiple PLL designs and worst-case PVT variations.

expression as described in [1]. A maximum limit can be placed on the power consumption of the PLL, or power can be chosen as the optimization objective. Repeating this constraint over multiple PVT scenarios guarantees that it will be satisfied in the worst-case condition.

B. VCO frequency range and saturation margins

The inverter delay in the VCO can be approximated by an effective transconductance divided by the total capacitance at each oscillating node. Therefore, the frequency of oscillation can be written in monomial form, $f = \frac{1}{2S}\frac{g_{\mathrm{m,osc}}}{C_{\mathrm{L,osc}}}$. In reality, this approximation is not sufficient. Both non-linear switching effects and parasitic routing capacitance must be considered for accurate frequency modeling in the 2GHz range. To solve this, GP compatible macromodels can be created for the frequency (f_{vco}), internal oscillator supply voltage (V_{d}), and gain ($\frac{\partial f_{\mathrm{vco}}}{\partial I_{\mathrm{ring}}}$) of the current controlled ring oscillator in terms of the design variables (W_{Mn}, L_{Mn}, I_{ring}, S, and C_{L}). These macromodels can be created by generating extracted simulation data over a wide range of each of the design variables, and fitting the data into a monomial form. Although not discussed here, the PLL layout can also be incorporated into the GP formulation. The load capacitance, C_{L}, includes an estimate of the parasitic routing capacitance between the VCO and the CNV. This is one example demonstrating how layout dependent parasitics are taken into account during the optimization.

Once accurate models for f_{vco} and V_{d} are known, saturation constraints determining the VCO frequency range can be written (ignoring body effect and switch resistance).

$$\begin{array}{c} V_d \leq V_{dd} - V_{gov,M3v} \\ \frac{1}{V_{dd}}\left(V_d + V_{gov,M3v}\right) \leq 1 \end{array} \tag{4}$$

$$\begin{array}{c} V_{gov,M1v} + V_{t,M1v} \leq V_{dd} - \left(V_{gov,M8d} + V_{t,M8d} - V_{t,M8c}\right) \\ \frac{1}{V_{dd}}\left(V_{gov,M1v} + V_{t,M1v} + V_{gov,M8d}\right) \leq 1 \end{array} \tag{5}$$

These posynomial inequalities keeping $M3v$ and $M8c$ in saturation will be tight at the maximum VCO frequency (*i.e.* $f_{\mathrm{vco}} = f_{\mathrm{vco,max}}$). Similar constraints are added for transistors $M1v$ and $M6c$. Repeating these constraints for the minimum VCO frequency (*i.e.* $f_{\mathrm{vco}} = f_{\mathrm{vco,min}}$) ensures that the saturation conditions will be met over the entire frequency range. In this way, the VCO frequency can be thought of as another scenario, analogous to PVT variations. In Fig. 4, extracted full-loop simulation results for the control voltage of the PLL ($V_{\mathrm{cntl}} = V_{\mathrm{gov,M1v}} + V_{\mathrm{t,M1v}}$) show the accuracy of these models over multiple designs, as well as over worst-case PVT and VCO frequency scenarios. In fact, all of the specifications in the PLL optimization are repeated over PVT and VCO frequency scenarios, ensuring that all of the specifications will be met in the worst-case conditions.

C. Accumulated jitter

For a second-order PLL dominated by intrinsic VCO noise, the variance of the accumulated jitter can be expressed as $\sigma_{\mathrm{j}}^2 = \kappa^2 \frac{1}{2\zeta\omega_{\mathrm{n}}}$, where ω_{n} is the natural frequency of the PLL and ζ is the damping factor [5]. Using a linear, time-variant oscillator noise model [6], κ_{osc} can be expressed as the following posynomial,

$$\kappa_{osc}^2 = \left(\frac{\Gamma_{rms}}{q_{max}\omega_{vco}}\right)^2 \frac{1}{2}\frac{\overline{i_n^2}}{\Delta f}, \tag{6}$$

where $\Gamma_{\mathrm{rms}} = \sqrt{\frac{2\pi^2}{3(0.75S)^3}}$, $q_{\mathrm{max}} = C_{\mathrm{L}}V_{\mathrm{d}}$, $\omega_{\mathrm{vco}} = 2\pi f_{\mathrm{vco}}$, and $\frac{\overline{i_{\mathrm{n}}^2}}{\Delta f} = 4kT\gamma\left(g_{\mathrm{m,Mn}} + g_{\mathrm{m,Mp}}\right)S$. The total equivalent κ includes contributions from the oscillator devices, as well as contributions from the voltage to current converter ($M1v$, $M2v$, and $M3v$) and the loop filter resistor (R) [7]:

$$\begin{aligned} \kappa^2 \quad &= \kappa_{osc}^2 + 4kTR\left(\frac{K_{vco}^2}{2\omega_{vco}^2}\right) + \left(\frac{\partial\omega_{\mathrm{vco}}}{\partial I_{\mathrm{ring}}}\right)^2\left(\frac{1}{2\omega_{vco}^2}\right) \\ &\quad 4kT\gamma\left[g_{m,M3v} + \left(\frac{W_{M3v}}{W_{M2v}}\right)^2\left(g_{m,M1v} + g_{m,M2v}\right)\right], \end{aligned} \tag{7}$$

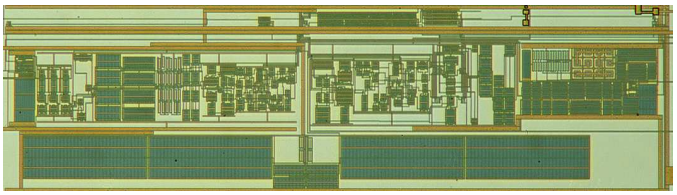

Fig. 5. Die photo showing one of six PLL circuits fabricated in a 0.18μm CMOS process.

where $K_{\rm vco} = g_{\rm m,M1v}\left(\frac{W_{\rm M3v}}{W_{\rm M2v}}\right)\left(\frac{\partial\omega_{\rm vco}}{\partial I_{\rm ring}}\right)$.

Monomial expressions for $\omega_{\rm n}$ and ζ of the PLL are shown below:

$$\omega_n = \sqrt{\frac{K_{pd}K_{cp}K_{vco}}{NPC_1}} \text{ and } \zeta = \frac{\omega_n RC_1}{2}, \qquad (8)$$

where $K_{\rm pd} = \frac{1}{2\pi}$, $K_{\rm cp} = I_{\rm ref}\left(\frac{W_{\rm M5c}}{W_{\rm M5b}}\right)$, $C_1 = C_{\rm ox}W_{\rm M1}L_{\rm M1}$, and NP is the total division ratio in the feedback path.

Combining (6), (7), and (8) with $\sigma_{\rm j}^2 = \kappa^2\frac{1}{2\zeta\omega_{\rm n}}$ results in a posynomial expression for accumulated jitter.

Posynomial inequalities for continuous and discrete time stability, non-linear acquisition time, static phase error, jitter due to power supply noise, and other key specifications are included in the GP problem formulation of the PLL, but are not shown here.

V. Silicon results for an optimized PLL array in 0.18μm CMOS

Optimizations were performed on a wide variety of PLL specifications in order to test the GP code. A typical optimization over all PVT and VCO frequency scenarios will take 5 to 12 hours on a 1GHz PC. An array of six of these PLL circuits was fabricated in a 0.18μm, 1.8V CMOS logic process. No manual modifications were made to any of the PLL circuits. A die photo showing the detail of one of the six fabricated PLL circuits is shown in Fig. 5.

Table I compares different optimization results against silicon measurements for the typical PVT scenario. Good agreement between power consumption and accumulated jitter is shown. The GP results for static phase error are pessimistic compared to the measurement. This is because accurate expressions do not exist for either channel charge injection of $M1c$ and $M3c$, or the magnitude and phase of the power supply noise at the PFD input frequency, $F_{\rm ref}$. Pessimistic approximations are used to handle both effects on static phase error.

Silicon measurements of the area, period jitter, and period jitter due to power supply noise from the PLL array are included in Table II. On-chip noise generation circuitry similar to [4] was included in order to measure jitter performance in response to a 10% step in voltage on the power supply, emulating a harsh digital environment. At the time these optimizations were performed, only rough approximations were completed for $T_{\rm pj}$ and $T_{\rm pj,noi}$, so that no GP prediction was available. In spite of this, $T_{\rm pj}$ results as low as 2.1ps and $T_{\rm pj,noi}$ results approaching $0.1\frac{\%_{\rm period,vco}}{\%{\rm V_{dd}}}$ are achieved.

TABLE I

GP prediction vs. silicon measurement for 0.18μm PLL array - $T_{\rm aj}$ is 1σ accumulated jitter. ($\Phi_{\rm e}$) is static phase error.

#	$F_{\rm ref}$ [MHz]	$F_{\rm vco}$ [MHz]	Power [mW]		$T_{\rm aj}$ [ps]		$\Phi_{\rm e}$ [ps]	
			GP	Meas	GP	Meas	GP	Meas
1	50	1200-1900	11.0	10.8	5.7	6.2	93	93
2	33	600-1600	8.8	7.3	7.5	8.0	90	62
3	10	1500	7.9	6.0	15.3	14.4	70	54
4	20	400	3.2	2.8	14.3	12.0	89	28
5	25	250	3.0	3.0	9.7	9.6	78	16
6	3-6	81-135	2.7	2.5	27.9	24.2	92	48

TABLE II

Silicon measurements of PLL array - $T_{\rm pj}$ is 1σ, $V_{\rm dd}$ clean period jitter. $T_{\rm pj,noi}$ is peak period jitter due to 10% $V_{\rm dd}$ step.

#	Minimize	Area [μm^2]	$T_{\rm pj}$ [ps]	$T_{\rm pj,noi}$ [ps, $\frac{\%_{\rm period,vco}}{\%{\rm V_{dd}}}$]
1	Area	970 x 525	2.2	58, 1.10
2	Area	935 x 450	2.1	41, 0.66
3	$T_{\rm pj,noi}$	1480 x 500	4.2	65, 0.98
4	Power	890 x 281	2.7	31, 0.12
5	Area	885 x 310	3.1	59, 0.15
6	Power	970 x 505	5.9	136, 0.18

VI. Conclusion

An efficient, systematic, and robust method for the optimization of PLL circuits using geometric programming has been illustrated. The optimization returns a DRC and LVS clean layout of a PLL. PLL circuits with VCO frequencies ranging from 81MHz to 1.9GHz were automatically generated using this technique. Power consumption predictions down to 3mW and accumulated jitter predictions below 6ps agree with silicon measurements. Using this technique, the PLL design cycle is reduced from a matter of weeks to a matter of hours. To the authors' knowledge, this is the first example of fully-automated PLL design.

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