Optimizing dominant time constant in RC circuits

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Abstract

We propose to use the *dominant time constant* of a resistor-capacitor (RC) circuit as a measure of the signal propagation delay through the circuit. We show that the dominant time constant is a quasiconvex function of the conductances and capacitances, and use this property to cast several interesting design problems as *convex optimization problems*, specifically, semidefinite programs (SDPs). For example, assuming that the conductances and capacitances are affine functions of the design parameters (which is a common model in transistor or interconnect wire sizing), one can minimize the power consumption or the area subject to an upper bound on the dominant time constant, or compute the optimal tradeoff surface between power, dominant time constant, and area. We will also note that, to a certain extent, convex optimization can be used to design the *topology* of the interconnect wires.

This approach has two advantages over methods based on Elmore delay optimization. First, it handles a far wider class of circuits, *e.g.*, those with non-grounded capacitors. Second, it always results in convex optimization problems for which very efficient interior-point methods have recently been developed.

We illustrate the method, and extensions, with several examples involving optimal wire and transistor sizing.

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1 Introduction

Determining the optimal dimensions of the transistors and interconnect wires in a digital circuit involves a tradeoff between signal delay, area, and power dissipation. The conventional approach to optimal sizing is based on linear RC models and on the *Elmore delay* as a measure of signal propagation delay. This approach finds its origins in the work of Elmore[Elm48], Rubinstein, Penfield and Horowitz[RPH83], and Fishburn and Dunlop[FD85]. In particular, Fishburn and Dunlop were first to observe that under certain conditions (the resistors form a tree with the input voltage source at its root and all capacitors are grounded) the Elmore delay of an RC circuit is a *posynomial function* of the conductances and capacitances. This observation has the important consequence that convex programming, specifically geometric programming, can be used to optimize Elmore delay, area, and power consumption. Geometric programming forms the basis of the TILOS program and of several extensions and related programs developed since then [FD85, HSFK89, SSVFD88, ME87, SRVK93, Sap96].

In this paper we propose to use the *dominant time constant* as an alternative to the Elmore delay. The resulting method has two important advantages over methods based on Elmore delay optimization. First, a far wider class of circuits can be handled, including for example circuits with capacitive coupling between the nodes. We will give an example that illustrates the practical significance of this extension. Second, the dominant time constant of a general RC circuit is a quasiconvex function of the design parameters, and it can be optimized using convex optimization techniques (specifically, semidefinite programming). The Elmore delay, on the other hand, leads to convex optimization problems only for a very special class of circuits (which excludes, for example, circuits with loops of resistors). Moreover practical experience suggests that the numerical values of Elmore delay and dominant time constant are usually close.

The method will be illustrated with five examples (Section 5). The first two of these examples (§5.1 and §5.2) are applications that can also be handled with classical Elmore delay optimization. They are included to show that, where they both apply, dominant time constant and Elmore delay minimization give very similar results. The next two examples (§5.3 and §5.4) are applications that cannot be handled using Elmore delay minimization because of the presence of resistor loops in the circuit. These two examples will illustrate that, to a certain extent, convex optimization can be used to design the *topology* of the interconnect wires. The fifth example (§5.5) is the best illustration of how much more general the new technique is. Here we simultaneously determine the optimal sizes of interconnect wires and the optimal distances between them, taking into account capacitive coupling between neighboring wires. We will see that optimizing dominant time constant allows us to control not only the signal propagation delay, but also indirectly the crosstalk between the wires. This is not possible with Elmore delay minimization, since the Elmore delay is only defined for circuits with grounded capacitors. This example is of practical importance in deep submicron technologies where the coupling capacitance can be significantly higher than the plate capacitance.

The outline of the rest of the paper is as follows. In §2 we describe the circuit model considered in the paper and the special cases that we will encounter. We also explain how these different RC circuit models arise in MOS transistor and interconnect wire sizing. In §3

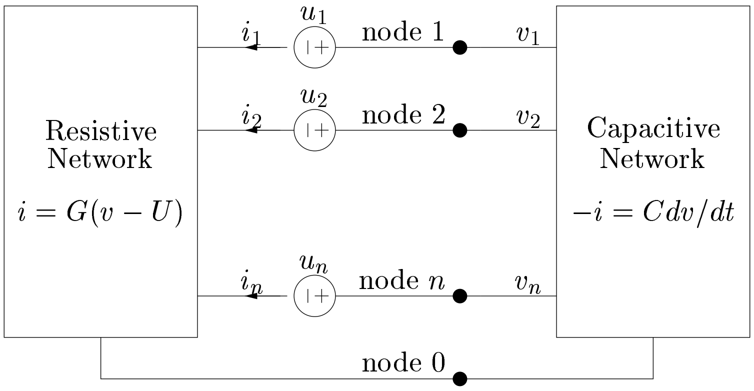

Figure 1: General RC circuit with $n+1$ nodes shown as a resistive network, a capacitive network, and voltages sources.

we discuss three definitions of signal propagation delay. In §4 we show that optimizing the dominant time constant leads to semidefinite programming problems, a special class of convex optimzation problems for which very efficient methods have recently been developed. Section 5 contains the five examples. In Section 6 we relate the three definitions of signal propagation delay. Section 7 gives a short discussion of the computational complexity.

2 Circuit models

2.1 General RC circuit

We consider linear resistor-capacitor (RC) circuits that can be described by the differential equation

$$C\frac{dv}{dt} = -G(v(t) - u(t)), \tag{1}$$

where $v(t) \in \mathbf{R}^n$ is the vector of node voltages, $u(t) \in \mathbf{R}^n$ is the vector of independent voltage sources, $C \in \mathbf{R}^{n\times n}$ is the capacitance matrix, and $G \in \mathbf{R}^{n\times n}$ is the conductance matrix (see Figure 1). Throughout this paper we assume that C and G are symmetric and positive definite (*i.e.*, that the capacitive and resistive subcircuits are reciprocal and strictly passive). In a few examples and the appendix we will also consider the case in which C and G are only positive semidefinite, *i.e.*, possibly singular.

We are interested in design problems in which C and G depend on some design parameters $x \in \mathbf{R}^m$. Specifically we assume that the matrices C and G are *affine* functions of x, *i.e.*,

$$C(x) = C_0 + x_1C_1 + \cdots + x_mC_m, \quad G(x) = G_0 + x_1G_1 + \cdots + x_mG_m, \tag{2}$$

where C_i and G_i are symmetric matrices.

We will refer to a circuit described by (1) and (2) as a *general RC circuit*. We will also consider several important special cases, for example circuits composed of two-terminal elements, circuits in which the resistive network forms a tree, or all capacitors are grounded. We describe these special cases now.

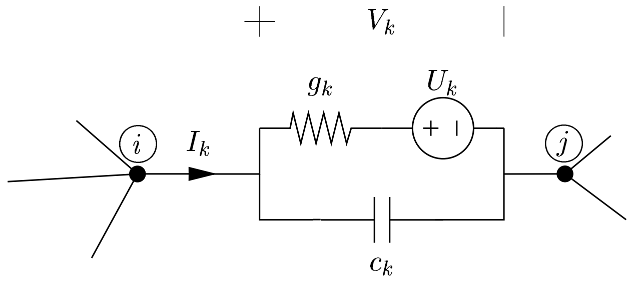

Figure 2: Orientation of the kth branch voltage V_k and branch current I_k in an RC circuit. Each branch consists of a capacitor $c_k \geq 0$, and a resistor with conductance $g_k \geq 0$ in series with an independent voltage source U_k.

2.2 RC circuit

When the general RC circuit is composed of two terminal resistors and capacitors (and the independent voltage sources) we will refer to it as an *RC circuit*. More precisely, consider a circuit with N branches and $n+1$ nodes, numbered 0 to n, where node 0 is the ground or reference node. Each branch k consists of a capacitor $c_k \geq 0$, and a conductance $g_k \geq 0$ in series with a voltage source U_k (see Figure 2). Some branches can have a zero capacitance or a zero conductance, but we will assume that both the capacitive subnetwork (*i.e.*, the network obtained by removing all resistors and voltage sources), and the resistive subnetwork (*i.e.*, the network obtained by removing all capacitors) are connected.

We denote the vector of node voltages by $v \in \mathbf{R}^n$, the vector of branch voltages by $V \in \mathbf{R}^N$ and the vector of branch currents by $I \in \mathbf{R}^N$. The relation between branch voltages and currents is

$$I_k = c_k \frac{dV_k}{dt} + g_k(V_k - U_k), \quad k = 1, \ldots, N. \tag{3}$$

To obtain a description of the form (1), we introduce the reduced node-incidence matrix $A \in \mathbf{R}^{n \times N}$ and define C and G as

$$C = A\,\mathbf{diag}(c)A^T, \quad G = A\,\mathbf{diag}(g)A^T. \tag{4}$$

Obviously, C and G are positive semidefinite. Both matrices are also nonsingular if the capacitive and resistive subnetworks are connected. To see this, suppose that $c_k > 0$ for $k = 1, \ldots, N_+$ and $c_k = 0$ for $k > N_+$. Then $C = A_+\mathbf{diag}(c_+)A_+^T$, where c_+ is the vector with the first N_+ components of c, and A_+ is the matrix formed by the first N_+ columns of A (*i.e.*, the reduced node-incidence matrix of the capacitive subnetwork). Since a reduced node-incidence matrix of a network is of full row rank if and only if the network is connected, A_+ must have rank n, and hence C must be positive definite. In a similar way one can show that G is positive definite if the resistive subnetwork is connected.

Using Kirchhoff's laws $AI = 0$ and $V = A^T v$, it is now straightforward to write the branch equations (3) as (1) with $u = G^{-1}A\,\mathbf{diag}(g)\,U$.

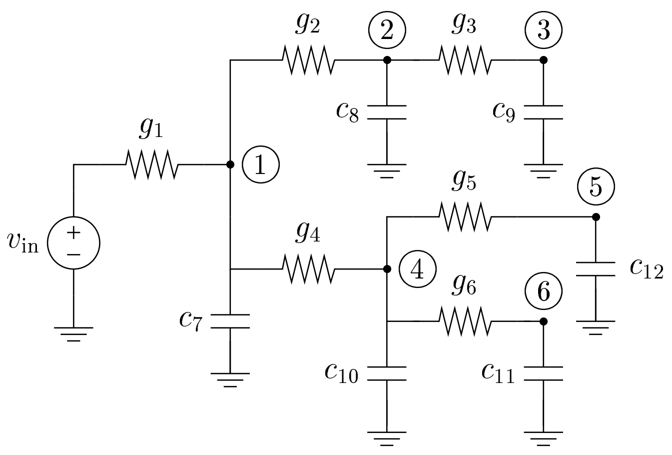

Figure 3: Example of a grounded capacitor RC tree.

For future use we note that for this class of circuits C and G have the following well-known form: for $i = 1, \ldots, n$,

$$G_{ii} = \sum_{k \in \mathcal{N}(i)} g_k, \quad C_{ii} = \sum_{k \in \mathcal{N}(i)} c_k,$$

where the summations extend over all branches connected to node i, and, for $i, j = 1, \ldots, n$, $i \neq j$,

$$G_{ij} = -\sum_{k \in \mathcal{N}(i,j)} g_k, \quad C_{ij} = -\sum_{k \in \mathcal{N}(i,j)} c_k$$

where the summations are over all branches between nodes i and j. In particular, the diagonal elements of C and G are positive and the off-diagonal elements are negative. It can also be shown that the matrices $R = G^{-1}$ and C^{-1} are elementwise nonnegative.

From the expressions for the matrices G and C (4), we see that they are affine functions of the design parameters x, if each of the conductances g_k and capacitances c_k is.

2.3 Grounded capacitor RC circuit

It is quite common that all capacitors in the RC circuit are connected to the ground node. In this case the matrix C is diagonal and nonsingular if there is a capacitor between every node and the ground. We will refer to circuits of this form as *grounded capacitor RC circuits.*

2.4 Grounded capacitor RC tree

The most restricted class of circuits considered in this paper consists of grounded capacitor RC circuits in which the resistive branches form a tree with the ground node as its root. Moreover only one resistive branch is connected to the ground node, and it contains the only voltage source in the circuit. An example is shown in Figure 3.

Note that the resistance matrix $R = G^{-1}$ for a circuit of this class can be written down by inspection:

$$R_{ij} = \sum \text{resistances upstream from node } i \text{ and node } j, \tag{5}$$

i.e., to find R_{ij} we add all resistances in the intersection of the unique path from node i to the root of the tree and the unique path from node j to the root of the tree. For the example in Figure 3, we obtain

$$R = \begin{bmatrix} r_1 & r_1 & r_1 & r_1 & r_1 & r_1 \\ r_1 & r_1+r_2 & r_1+r_2 & r_1 & r_1 & r_1 \\ r_1 & r_1+r_2 & r_1+r_2+r_3 & r_1 & r_1 & r_1 \\ r_1 & r_1 & r_1 & r_1+r_4 & r_1+r_4 & r_1+r_4 \\ r_1 & r_1 & r_1 & r_1+r_4 & r_1+r_4+r_6 & r_1+r_4 \\ r_1 & r_1 & r_1 & r_1+r_4 & r_1+r_4 & r_1+r_4+r_5 \end{bmatrix}$$

where $r_i = 1/g_i$.

One can also verify that in a grounded capacitor RC tree with input voltage $v_{\text{in}}(t)$, the vector $u(t)$ in (1) is equal to $u(t) = v_{\text{in}}(t)e$ where e is the vector with all components equal to one.

2.5 Applications

Linear RC circuits are often used as approximate models for transistors and interconnect wires. When the design parameters are the physical widths of conductors or transistors, the conductance and capacitance matrices are affine in these parameters, *i.e.*, they have the form (2).

An important example is wire sizing, where x_i denotes the width of a segment of some conductor or interconnect line. A simple lumped model of the segment consists of a π section: a series conductance, with a capacitance to ground on each end. Here the conductance is linear in the width x_i, and the capacitances are linear or affine. We can also model each segment by many such π sections, and still have the general form (1), (2).

Another important example is an MOS transistor circuit where x_i denotes the width of a transistor. When the transistor is 'on' it is modeled as a conductance that is proportional to x_i, and a source-to-ground capacitance and drain-to-ground capacitance that are linear or affine in x_i.

3 Delay

We are interested in how fast a change in the input u propagates to the different nodes of the circuit, and in how this propagation delay varies as a function of the resistances and capacitances. In this section we introduce three possible measures for this propagation delay: the threshold delay, which is the most natural measure but difficult to handle mathematically; the Elmore delay, which is widely used in transistor and wire sizing; and the dominant time constant. We will compare the three delay measures in the examples of §5 where we will observe that their numerical values are usually quite close. More theoretical details on the relation between these three measures will be presented in §6, including some bounds that they must satisfy.

We assume that for $t < 0$, the circuit is in static steady-state with $u(t) = v(t) = v_-$. For $t \geq 0$, the source switches to the constant value $u(t) = v_+$. As a result we have, for $t \geq 0$,

$$v(t) = v_+ + e^{-C^{-1}Gt}(v_- - v_+) \tag{6}$$

which converges, as $t \to \infty$, to v_+ (since our assumption $C > 0$, $G > 0$ implies stability). The difference between the node voltage and its ultimate value is given by

$$\tilde{v}(t) = e^{-C^{-1}Gt}(v_- - v_+),$$

and we are interested in how large t must be before this is small.

To simplify notation, we will relabel $\tilde{v}$ as v, and from here on study the rate at which

$$v(t) = e^{-C^{-1}Gt}v(0) \tag{7}$$

becomes small. Note that this v satisfies the autonomous equation $Cdv/dt = -Gv$.

It can be shown that for a grounded capacitor RC circuit the matrix $e^{-C^{-1}Gt}$ is elementwise nonnegative for all $t \geq 0$ (see Berman and Plemmons[BP94, Theorem 3.12]). Therefore, if $v(0) \geq 0$ (meaning, $v_k(0) \geq 0$ for $k = 1, \ldots, n$) in (7), the voltages remain nonnegative, *i.e.*, for $t \geq 0$ we have

$$v(t) \geq 0.$$

Also note that in a grounded capacitor RC tree, the steady-state node voltages are all equal. When discussing RC trees, we will therefore assume without loss of generality that the input switches from zero to one at $t = 0$, *i.e.*, $v_- = 0$, $v_+ = e$ in (6), or, for the autonomous model, that $v(0) = e$ in (7).

3.1 Threshold delay

In many applications the natural measure of the delay at node k is the first time after which v_k stays below some given threshold level $\alpha > 0$, *i.e.*,

$$T_k^{\text{thres}} = \inf\{ \, T \mid |v_k(t)| \leq \alpha \text{ for } t \geq T \, \}.$$

We will call the maximum threshold delay to any node the *critical threshold delay* of the circuit:

$$T^{\text{thres}} = \max\{T_1^{\text{thres}}, \ldots, T_n^{\text{thres}}\} = \inf\{ \, T \mid \|v(t)\|_\infty \leq \alpha \text{ for } t \geq T \, \},$$

where $\|\cdot\|_\infty$ denotes the infinity norm, defined by $\|z\|_\infty = \max_i |z_i|$. The critical threshold delay is the first time after which all node voltages are less than α.

The critical threshold delay T^{thres} depends on the design parameters x through (7), *i.e.*, in a very complicated way. Methods for direct optimization of T^{thres} are inefficient and also local, *i.e.*, not guaranteed to find a globally optimal design.

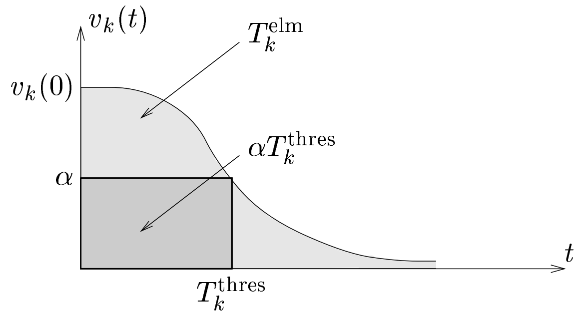

Figure 4: *Graphical interpretation of the Elmore delay at node k.* T_k^{thres} is the threshold delay at node k. The area below v_k, which is shaded lightly, is T_k^{elm}. The darker shaded box, which lies below v_k, has area $\alpha T_k^{\text{thres}}$. From this it is clear that when the voltage is nonnegative and monotonically decaying, $\alpha T_k^{\text{thres}} \leq T_k^{\text{elm}}$.

3.2 Elmore delay

In[Elm48], Elmore introduced a measure of the delay to a node that depends on C and G (hence, x) in a simpler way than the threshold delay, and often gives an acceptable approximation to it. The Elmore delay to node k is defined as

$$T^{\text{elm}} = \int_0^\infty v_k(t)\, dt.$$

While T_k^{elm} is always defined, it can be interpreted as a measure of delay only when $v_k(t) \geq 0$ for all $t \geq 0$, *i.e.*, when the node voltage is nonnegative. (Which is the case, as we mentioned, in grounded capacitor RC circuits with $v(0) \geq 0$.)

In the common case that the voltages decay monotonically, *i.e.*, $dv_k(t)/dt \leq 0$ for all $t \geq 0$, we have the simple bound

$$\alpha T^{\text{thres}} \leq T_k^{\text{elm}},$$

which can be derived as follows. Assuming v_k is positive and nonincreasing, we must have $v_k(t) > \alpha$ for $t < T_k^{\text{thres}}$. Hence the integral of v_k must exceed $\alpha T_k^{\text{thres}}$ (see Figure 4). The monotonic decay property holds, for example, for grounded capacitor RC trees (see [RPH83, Appendix C]).

We can express the Elmore delay in terms of G, C, and $v(0)$ as

$$T_k^{\text{elm}} = e_k^T G^{-1} C v(0)$$

where e_k is the kth unit vector. Thus the vector of Elmore delays is given by the simple expression $RCv(0)$, where $R = G^{-1}$ is the resistance matrix. We define the *critical Elmore delay* as the largest Elmore delay at any node, *i.e.*, $T^{\text{elm}} = \max_k T_k^{\text{elm}}$.

For a grounded capacitor RC circuit with $v(0) \geq 0$ we can express the critical Elmore delay as

$$T^{\text{elm}} = \|G^{-1} C v(0)\|_\infty,$$

by noting that the matrix $G^{-1}C = RC$ is elementwise nonnegative. If $v(0) = e$ (as in a grounded-capacitor RC tree) we can also write

$$T^{\text{elm}} = \max_k \left(e_k^T G^{-1} C e \right) = \|G^{-1} C\|_\infty. \tag{8}$$

(For a matrix $A \in \mathbf{R}^{n\times n}$, $\|A\|_\infty$ is the maximum row sum of A, *i.e.*, $\|A\|_\infty = \max_{i=1,\dots,n} \sum_{j=1}^n |A_{ij}|$.)

3.3 Dominant time constant

In this paper we propose using the *dominant time constant* of the RC circuit as a measure of the delay. We start with the definition. Let $\lambda_1, \dots, \lambda_n$ denote the eigenvalues of the circuit, *i.e.*, the eigenvalues of $-C^{-1}G$, or equivalently, the roots of the characteristic polynomial $\det(sC+G)$. They are real and negative since they are also the eigenvalues of the symmetric, negative definite matrix

$$C^{1/2}\left(-C^{-1}G\right)C^{-1/2} = -C^{-1/2}GC^{-1/2}$$

(which is similar to $-C^{-1}G$). We assume they are sorted in decreasing order, *i.e.*,

$$0 > \lambda_1 \geq \cdots \geq \lambda_n.$$

The largest eigenvalue, λ_1, is called the *dominant eigenvalue* or *dominant pole* of the RC circuit.

Each node voltage can be expressed in the form

$$v_k(t) = \sum_{i=1}^n \alpha_{ik} e^{\lambda_i t}, \tag{9}$$

which is a sum of decaying exponentials with rates given by the eigenvalues. We define the *dominant time constant* at the kth node as follows. Let p denote the index of the first nonzero term in the sum (9), *i.e.*, $\alpha_{ik} = 0$ for $i < p$ and $\alpha_{ip} \neq 0$. (Thus, the slowest decaying term in v_k is $\alpha_{ip}e^{\lambda_p t}$.) We call λ_p the *dominant eigenvalue* at node k, and the dominant time constant at node k is defined as

$$T_k^{\mathrm{dom}} = -1/\lambda_p.$$

In most cases, v_k contains a term associated with the largest eigenvalue λ_1, in which case we simply have $T_k^{\mathrm{dom}} = -1/\lambda_1$.

The dominant time constant T_k^{dom} measures the asymptotic rate of decay of $v_k(t)$, and there are several ways to interpret it. For example, T_k^{dom} is the smallest number T such that

$$|v_k(t)| \leq \beta e^{-t/T}$$

holds for some β and all $t \geq 0$.

The *(critical) dominant time constant* is defined as $T^{\mathrm{dom}} = \max_k T_k^{\mathrm{dom}}$. Except in the pathological case when $v(0)$ is deficient in the eigenvector associated with λ_1, we have

$$T^{\mathrm{dom}} = -1/\lambda_1. \tag{10}$$

In the sequel we will assume this is the case.

Note that the dominant time constant T^{dom} is a very complicated function of G and C, *i.e.*, the negative inverse of the largest zero of the polynomial $\det(sC+G)$. The dominant time constant can also be expressed in another form that will be more useful to us:

$$T^{\mathrm{dom}} = \min\{\ T \mid TG - C \geq 0\ \}.$$

This form has another advantage: it makes sense and provides a reasonable measure of delay in the case when C and G are only positive semidefinite (*i.e.*, possibly singular). We will see this in several of the examples; the details are given in Appendix A.

4 Dominant time constant optimization

In this section we show how several important design problems involving dominant time constant, area, and power, can be cast as convex or quasiconvex optimization problems that can be solved very efficiently.

4.1 Dominant time constant specification as linear matrix inequality

The dominant pole λ_1 can be expressed as

$$\lambda_1 = \inf\{\lambda \mid \lambda C(x) + G(x) \geq 0\}, \tag{11}$$

and hence, in particular, $\lambda_1 C(x) + G(x) \geq 0$. Another consequence of (11) is

$$T^{\mathrm{dom}}(x) \leq T_{\max} \Longleftrightarrow T_{\max} G(x) - C(x) \geq 0. \tag{12}$$

This type of constraint is called a *linear matrix inequality* (LMI): the left hand side is a symmetric matrix, the entries of which are affine functions of x. It can be shown that the set of vectors x that satisfy (12) is convex.

We conclude that T^{dom} is a *quasiconvex* function of x, *i.e.*, its sublevel sets

$$\left\{x \;\middle|\; T^{\mathrm{dom}}(x) \leq T_{\max}\right\}$$

are convex sets for all $T_{\max}$. Quasiconvexity can also be expressed as: for $\theta \in [0, 1]$,

$$T^{\mathrm{dom}}(\theta x + (1-\theta)\tilde{x}) \leq \max\{T^{\mathrm{dom}}(x), T^{\mathrm{dom}}(\tilde{x})\},$$

i.e., as the design parameters vary on a segment between two values, the dominant time constant is never any more than the largest of the two dominant time constants at the endpoints.

Linear matrix inequalities have recently been recognized as an efficient and unified representation of a wide variety of nonlinear convex constraints. They arise in many different fields such as control theory and combinatorial optimization (for surveys, see [BEFB94, NN94, VB96, LO96, Ali95]). Most importantly for us, many convex and quasiconvex optimization problems that involve LMIs can be solved with great efficiency using recently developed interior-point methods.

4.2 Optimization over LMIs

Here we briefly describe several common convex and quasiconvex optimization problems over LMIs.

The most common problem is *semidefinite programming* (SDP), in which we minimize a linear function subject to a linear matrix inequality:

$$\begin{array}{ll} \text{minimize} & c^T x \\ \text{subject to} & A(x) \geq 0, \end{array} \tag{13}$$

where $A(x) = A_0 + x_1A_1 + \cdots + x_mA_m$, $A_i = A_i^T$. Semidefinite programs are convex optimization problems, and can be solved very efficiently (see, *e.g.*, [NN94, VB96]). Some public domain general-purpose SDP software packages are SP[VB94], SDPSOL[WB96], and LMITOOL[END95].

We can handle multiple LMI constraints in SDP (13) by representing them as one big block diagonal matrix. We can also incorporate a wide variety of convex constraints on x by representing them as LMIs. For example, we can represent an SDP with additional linear inequalities on x,

$$\begin{array}{ll} \text{minimize} & c^T x \\ \text{subject to} & A(x) \geq 0 \\ & f_i^T x \leq g_i, \quad i = 1, \ldots, p \end{array} \tag{14}$$

as the SDP

$$\begin{array}{ll} \text{minimize} & c^T x \\ \text{subject to} & \left[\begin{array}{cc} A(x) & 0 \\ 0 & \mathbf{diag}(g_1 - f_1^T x, \ldots, g_p - f_p^T x) \end{array} \right] \geq 0. \end{array} \tag{15}$$

In the sequel we will simply refer to a problem such as (14), which is easily transformed to an SDP in the standard form (13), as an SDP.

Another common problem has the form

$$\begin{array}{ll} \text{minimize} & \lambda \\ \text{subject to} & \lambda B(x) - A(x) \geq 0 \\ & B(x) > 0, \quad C(x) \geq 0, \end{array} \tag{16}$$

where A, B, and C are symmetric matrices that are affine functions of x, and the variables are x and $\lambda \in \mathbf{R}$. This problem is called the *generalized eigenvalue minimization problem* (GEVP). GEVPs are quasiconvex and can be solved very efficiently using recently developed interior-point methods. See Boyd and El Ghaoui [BE93], Haeberly and Overton [HO94], and Nesterov and Nemirovsky [NN94, NN95, Nem94] for details on specialized algorithms.

4.3 Minimum area subject to bound on delay

We now return to circuit optimization problems. We suppose the area of the circuit is a linear (or affine) function of the variables x_i. This occurs when the variables represent the widths of transistors or conductors (with lengths fixed as l_i), in which case the circuit area has the form

$$a_0 + x_1 l_1 + \cdots + x_m l_m$$

where a_0 is the area of the fixed part of the circuit.

We can minimize the area subject to a bound on the dominant time constant $T^{\text{dom}} \leq T_{\max}$, and subject to upper and lower bounds on the widths by solving the SDP

$$\begin{array}{ll} \text{minimize} & \sum_{i=1}^{m} l_i x_i \\ \text{subject to} & T_{\max} G(x) - C(x) \geq 0 \\ & x_{\min} \leq x_i \leq x_{\max}, \quad i = 1, \ldots, m. \end{array} \tag{17}$$

By solving this SDP for a sequence of values of $T_{\max}$, we can compute the exact optimal tradeoff between area and dominant time constant. The optimal solutions of (17) are on the tradeoff curve, *i.e.*, they are *Pareto optimal* for area and dominant time constant.

4.4 Minimum power dissipation subject to bound on delay

The total energy dissipated in the resistors during a transition from initial voltage $\overline{v}$ to final voltage 0 (or between 0 and $\overline{v}$) is the energy stored in the capacitors, *i.e.*, $(1/2)\overline{v}^T C\overline{v}$. Therefore for a fixed clock rate and fixed probability of transition, the average power dissipated in proportional to

$$\overline{v}^T C(x)\overline{v} = \sum_{i=1}^{m} x_k \left(\overline{v}^T C_i \overline{v}\right),$$

which is a linear function of the design parameters x.

Therefore we can minimize power dissipation subject to a constraint on the dominant time constant by solving the SDP

$$\begin{array}{ll} \text{minimize} & \overline{v}^T C\overline{v} \\ \text{subject to} & T_{\max} G(x) - C(x) \geq 0 \\ & x_{\min} \leq x_i \leq x_{\max}, \quad i = 1, \ldots, m. \end{array}$$

We can also add an upper bound on area, which is a linear inequality. By solving this SDP for a sequence of values of $T_{\max}$, we can compute the optimal tradeoff between power dissipation and dominant time constant. By adding a constraint that the area cannot exceed $A_{\max}$, and solving the SDP for a sequence of values of $T_{\max}$ and $A_{\max}$, we can compute the exact optimal tradeoff surface between power dissipation, area, and dominant time constant.

4.5 Minimum delay subject to area and power constraints

We can also directly minimize the delay subject to limits on area and power dissipation, by solving the GEVP

$$\begin{array}{ll} \text{minimize} & T \\ \text{subject to} & TG(x) - C(x) \geq 0 \\ & x_{\min} \leq x_i \leq x_{\max}, \quad i = 1, \ldots, m \\ & f_i^T x \leq g_i, \quad i = 1, 2 \end{array}$$

with variables x and T, where the linear inequalities limit area and power dissipation.

4.6 Comparison with Elmore delay optimization

We briefly describe how Elmore delay can be optimized, in order to compare it with the methods for dominant time constant optimization we have described above.

Elmore delay is optimized only in a very special case: grounded capacitor RC trees where each conductance is proportional to exactly one variable. From (5) and (8) we see that the Elmore delay to node k can be written in the form

$$T_k^{\text{elm}} = \sum_{ij} \gamma_{ij} c_i / g_j \tag{18}$$

where the coefficients γ_{ij} are either zero or one. For example the Elmore delay to the third node of the circuit in Figure 3 is

$$T_3^{\mathrm{elm}} = c_9(r_1 + r_2 + r_3) + c_8(r_1 + r_2) + c_7 r_1 + c_{10} r_1 + c_{12} r_1 + c_{11} r_1.$$

Suppose each c_i is affine in the variable x, and each g_i is proportional to exactly one variable. Then (18) simplifies to a function of the form

$$f(x_1, \ldots, x_n) = \sum_{j=1}^{N} \beta_j \prod_{i=1}^{m} x_i^{\alpha_{ij}}. \tag{19}$$

where the coefficients β_j are nonnegative and the exponents α_{ij} can be -1, 0, or $+1$. A function of the form (19) (with α_{ij} arbitrary real numbers) is called a *posynomial* function, and an optimization problem of the form

$$\begin{array}{ll} \text{minimze} & f_0(x) \\ \text{subject to} & f_i(x) \leq 1, \quad i = 1, \ldots, n \\ & x > 0, \end{array} \tag{20}$$

where all functions f_i are posynomial, is called a *geometric programming* problem. Geometric programming problems can be cast as convex optimization problems by the following simple change of variables. Defining $y_i = \log x_i$, and expressing the function (19) in terms of y, we obtain

$$f(e^{y_1}, \ldots, e^{y_m}) = \sum_j \beta_j \exp\left(\sum_{i=1}^{m} \alpha_{ij} y_i\right),$$

which is convex in y. Applying this transformation to each of the functions in (20) yields a convex optimization problem in the variables y.

This fact was exploited in the TILOS program of Fishburn and Dunlop[FD85] for Elmore delay minimization, and in several more recent approaches to Elmore delay minimization in transistor and wire sizing (for examples, see [SSVFD88, HNSLS90, SRVK93, Sap96]).

We conclude this section by listing some limitations of the Elmore delay, and contrasting them with the dominant time constant. The main difference is that the dominant time constant *always* leads to tractable convex or quasiconvex optimization problems, with no restrictions on circuit topology. In particular:

- The circuits may contain loops of resistors. Although for grounded capacitor RC circuits with loops of resistors, the Elmore delay is still a meaningful approximation of signal delay (see Lin and Mead[LM84] and Wyatt[Wya85, Wya87]), it does not have a simple posynomial form as it does for RC trees, and convex optimization cannot be used to minimize it.

- The circuits may contain non grounded capacitors (*i.e.*, the matrix C in (1) may be nondiagonal). As we have seen, the voltages $v_k(t)$ can be negative in this case, and the Elmore delay is not a good measure for signal delay.

- Elmore delay gives the delay from one input node to one output node. The dominant time constant applies also to circuits with multiple input voltages.

- The Elmore delay in an RC tree is a posynomial function if the conductances depend on one variable only. For dominant time constant optimization the conductance and capacitances can be general affine functions of the variables.

The examples in the next section will illustrate these differences. The first two are applications to which Elmore delay would also apply, with very similar results. The third and fourth example illustrate the application to circuits with loops of resistors. The fifth example has non-grounded capacitors.

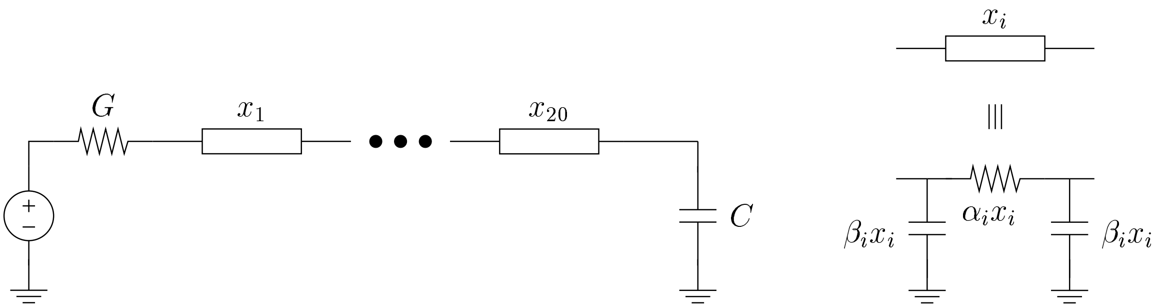

Figure 5: *Optimal wire sizing.* A voltage source and conductance drive a capacitor through a wire modeled as 20 π-segments with (fixed) lengths l_i and widths (to be designed) x_i.

5 Examples

5.1 Wire sizing

In the first example we consider the problem of sizing an interconnect wire that connects a voltage source and conductance G to a capacitive load C. We divide the wire into 20 segments of length l_i, and width x_i, $i = 1, \ldots, 20$, which is constrained as $0 \leq x_i \leq W_{\max}$. (We include this constraint just to show that it is readily handled.) The total area of the interconnect wire is therefore $\sum_i l_i x_i$. We use a π model of each wire segment, with capacitors $\beta_i x_i$ and conductance $\alpha_i x_i$. This is shown in Figure 5.

We used the following parameter values in our numerical simulation:

$$G = 1.0, \quad C = 10, \quad l_i = 1, \quad \alpha_i = 1.0, \quad \beta_i = 0.5, \quad W_{\max} = 1.$$

To minimize the total area subject to the width bound and a bound $T_{\max}$ on dominant time constant, we solve the SDP

$$\begin{array}{ll} \text{minimize} & \sum_{i=1}^{20} l_i x_i \\ \text{subject to} & T_{\max} G(x) - C(x) \geq 0 \\ & 0 \leq x_i \leq W_{\max}, \quad i = 1, \ldots, 20. \end{array}$$

By solving this SDP for a sequence of values of $T_{\max}$ that range between 300 and 2000, we can compute the optimal area-delay tradeoff for this example, which is shown in Figure 6. We emphasize that the tradeoff curve shown is the absolute tradeoff curve between the competing objectives, *i.e.*, area and dominant time constant. This is a consequence of the guaranteed global optimality of the solutions computed using semidefinite programming.

The general shape of the tradeoff curve is not a surprise: by increasing total area, we can reduce the dominant time constant. In this case the optimal tradeoff curve happens to be approximately hyperbolic, *i.e.*, it is approximately described by

$$\text{area} \cdot T^{\text{dom}} \approx 5000.$$

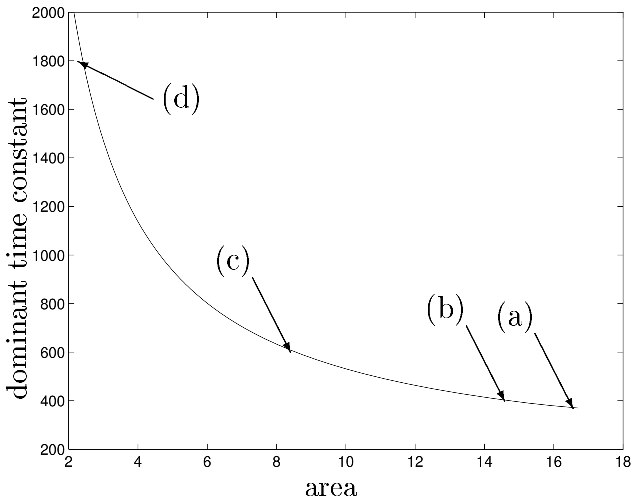

Figure 6: *Area-delay tradeoff curve.* The curve shows the (globally) optimal tradeoff curve between two competing objectives: the total area of the wire and the dominant time constant of the circuit. The solution for the four points marked on the curve is shown in Figure 7.

(the minimum value of the area-delay product is 4700 and the maximum value is 6180).

Figure 7 shows the solution x at the four points marked on the tradeoff curve. The general shape of these plots match what we would expect. The interconnect wire decreases in size as we move from the drive end towards the other end, since less current is needed to charge or discharge the capacitances farther down the line. As expected, this effect is more pronounced in the large, fast design (a), and much less evident in the small, slow design (d). We can see that the wire width limit becomes active only when the dominant time constant specification is smaller than 400 (or equivalently, the total area exceeds 14.5).

Figure 8 shows the step responses at the 21 nodes along the wire, for the two solutions marked (a) and (d) on the tradeoff curve. Note that in design (d) the voltage at the first nodes along the wire increases faster than in design (a), while the response at the end of the wire is much slower. This is easily explained. Since the capacitors in design (d) are much smaller than in (a), the voltage at the first nodes increases faster than in (a). However, since the resistances along the wire are larger in (d), the voltages at the last stages increase much more slowly. The dashed lines indicate the dominant time constant and the Elmore and 50%-threshold delays at the end node. We see that in both cases the dominant time constant is a reasonable approximation of the 0.5-threshold delay, and that T^{elm} and T^{dom} are very close.

Finally, note that the circuit is a grounded capacitor RC tree, and therefore the same designs could be done using Elmore delay instead of dominant time constant. In this example, simple wire sizing via dominant time constant optimization seems to produce results very close to wire sizing via Elmore delay optimization.

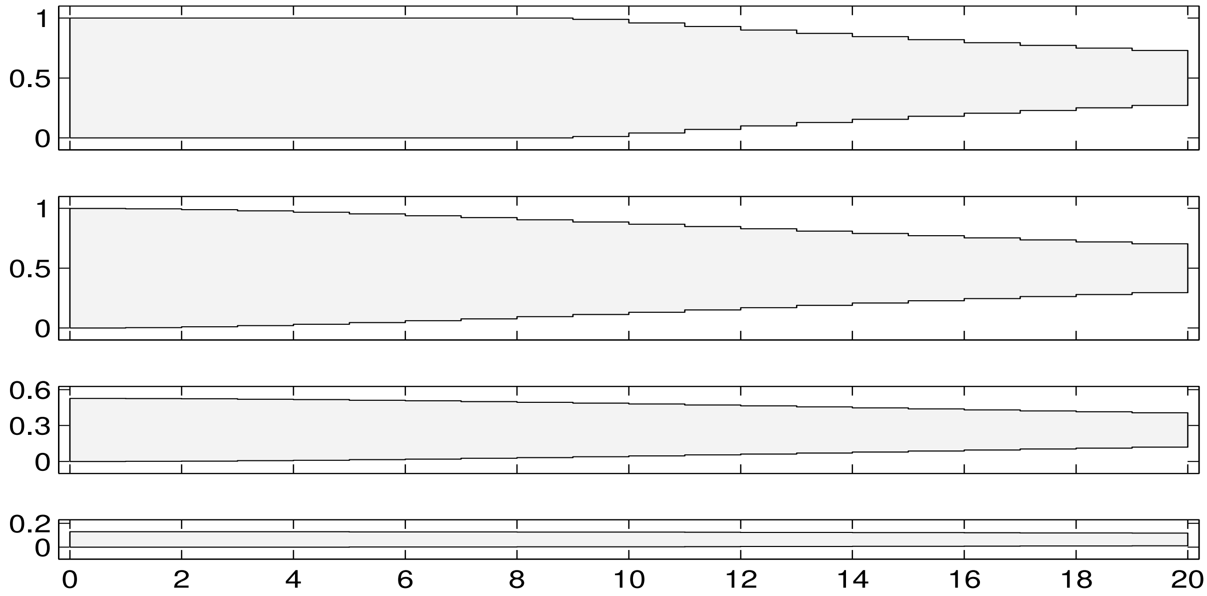

Figure 7: *Solution at four points on the tradeoff curve.* The top figure is the solution (a). The bottom figure is solution (d). The plots show wire width as a function of position. Each segment has unit length.

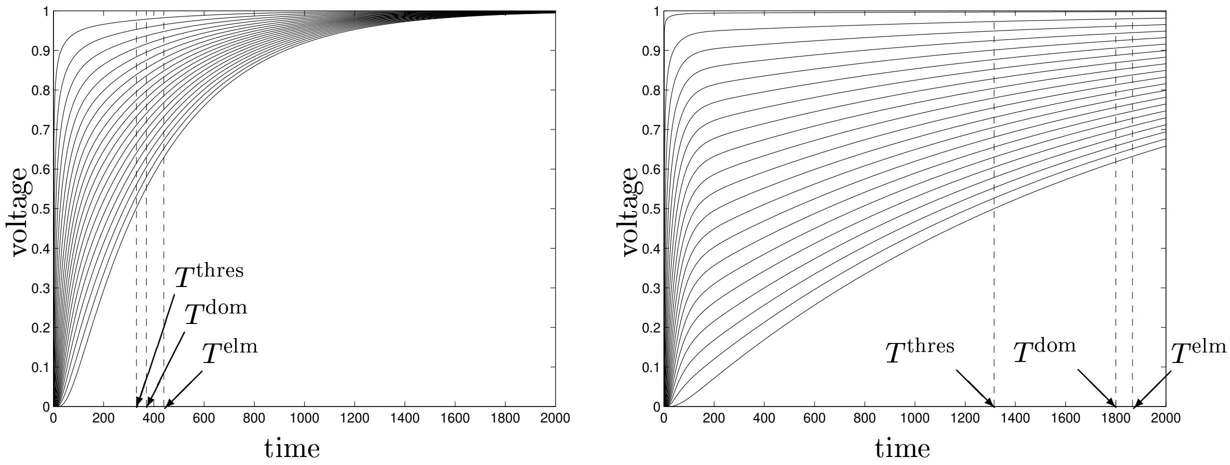

Figure 8: *Step responses at the 21 nodes. Left.* Step responses for the solution marked (a). *Right.* Step responses for the solution marked (d). The vertical lines show $T^{\rm thres}$, the 50% threshold delay (*i.e.*, $\alpha = 0.5$) at the output node, $T^{\rm dom}$, the dominant time constant, and $T^{\rm elm}$, the Elmore delay.

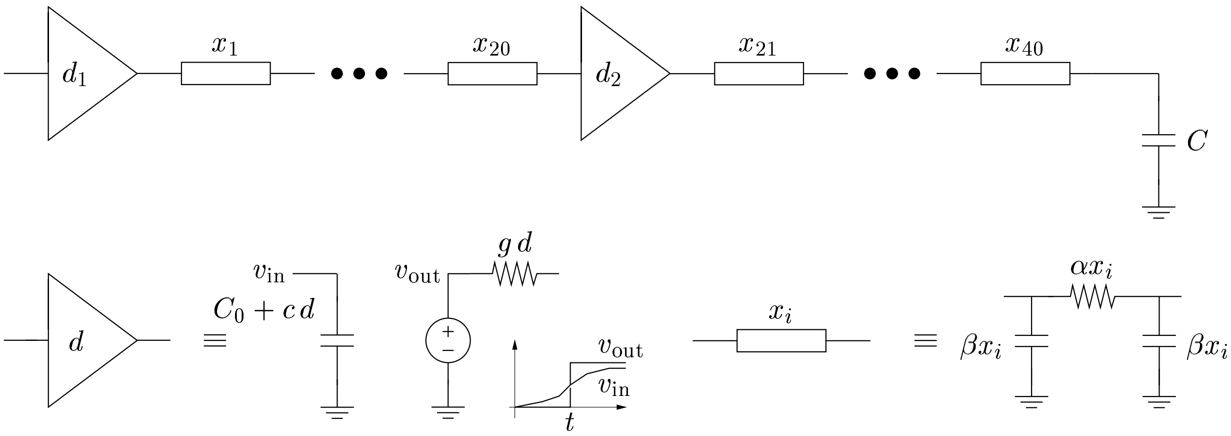

Figure 9: *Optimization of wire and repeater sizes.* The lefthand driver drives an interconnect wire, modeled as 20 RC π segments connected to a repeater, which drives a capacitive load through another 20 segment wire. The problem is to determine the sizes of the wire segments ($x_1, \ldots, x_{40}$) as well as the sizes of the driver and repeater d_1 and d_2.

5.2 Combined sizing of drivers, repeaters, and wire

Figure (9) depicts two repeaters inserted in an interconnect wire. The wires are divided in 20 segments each. The segments are modeled as π-segments with capacitance and conductance proportional to the segment widths. The dimensions of a repeater are characterized by one number d. The input capacitance of the repeater is affine in d: $C_0 + cd$; the output conductance is linear in d: gd. For the dynamics of the repeater we use a simplified model and assume that the output of the repeater is a perfect step input triggered when the input crosses a certain threshold. In this example we assume that the output of the first repeater is a perfect unit step at time $t = 0$ and that the output of the second repeater is a unit step at $t = T_1^{\mathrm{dom}}$, where T_1^{dom} is the dominant time constant of the first stage. We assume that the total area is equal to $L(d_1 + d_2) + \sum_{i=1}^{40} l_i x_i$, where l_i is the length of the ith segment, and $L(d_1 + d_2)$ is the area of the drivers.

The numerical values used in the calculations are

$$g = 1, \quad C_0 = 1, \quad c = 3, \quad \alpha = 5, \quad \beta = 0.1, \quad C = 50, \quad l_i = 1, \quad L = 10.$$

We also impose a maximum wire width of 2.

We want to minimize area subject to bound on the combined delay $T_1^{\mathrm{dom}} + T_2^{\mathrm{dom}}$ of the two stages. However, the sum of two quasiconvex functions is not quasiconvex, and therefore, minimizing the total area subject to a bound on $T_1^{\mathrm{dom}} + T_2^{\mathrm{dom}}$ is not a convex optimization problem. A reasonable sub-optimal solution consists in dividing the total allowed delay equally over the two stages. In other words we will replace the nonconvex constraint $T_1^{\mathrm{dom}} + T_2^{\mathrm{dom}} \le T_{\max}$ by two convex constraints

$$T_1^{\mathrm{dom}} \le T_{\max}/2, \quad T_2^{\mathrm{dom}} \le T_{\max}/2.$$

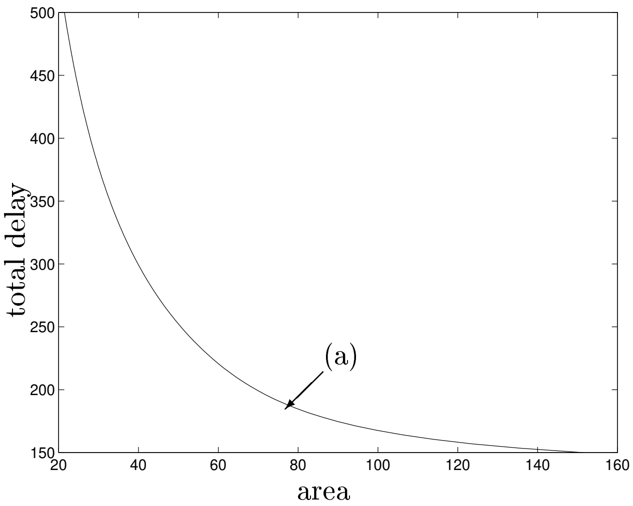

Figure 10: *Area-delay tradeoff.* The area is $10(d_1 + d_2) + \sum_i x_i$. The delay is equally distributed over the two stages, *i.e.*, total delay less than $T_{\max}$ means that $T_1^{\text{dom}} \leq T_{\max}/2$ and $T_2^{\text{dom}} \leq T_{\max}/2$, where T_1^{dom} and T_2^{dom} are the dominant time constants of the first and second stage, resp. The solution marked (a) is shown in Figure 11.

This leads to the optimization problem

$$\begin{array}{ll} \text{minimize} & L(d_1 + d_2) + \sum_{i=1}^{40} l_i x_i \\ \text{subject to} & 0 \leq x_i \leq 2, \quad i = 1, \ldots, 40 \\ & d_1, d_2 \geq 0 \\ & (T_{\max}/2)(G_1(x, d_1, d_2) - C_1(x, d_2) \geq 0 \\ & (T_{\max}/2)(G_2(x, d_2) - C_2(x) \geq 0, \end{array} \tag{21}$$

where $G_1 \in \mathbf{R}^{21 \times 21}$ is the conductance matrix of stage 1, $C_1 \in \mathbf{R}^{21 \times 21}$ is a diagonal matrix with the total capacitance at the nodes of stage 1 as its elements, $G_2 \in \mathbf{R}^{21 \times 21}$ is the conductance matrix of stage 2 and $C_2 \in \mathbf{R}^{21 \times 21}$ is a diagonal matrix with the total capacitance at the nodes of stage 2 as its elements.

Note that the two stages are almost uncoupled; only the size of the second repeater (d_2) couples the two stages, since it varies the capacitive load on the end of the first wire, and also determines the drive conductance for the second wire.

The tradeoff curve computed by solving the SDP (21) for a sequence of values $T_{\max}$ is shown in Figure 10. The solution marked (a) is shown in Figures 11 and 12.

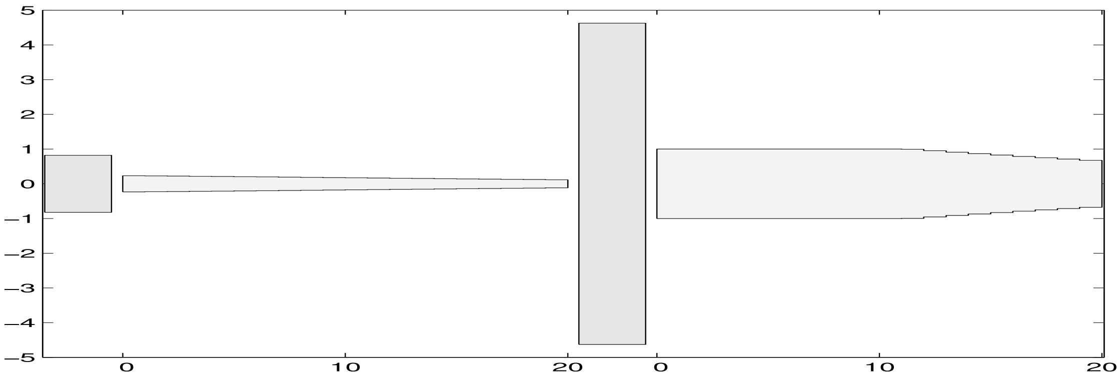

Figure 11: *Solution for the point on the tradeoff curve.* Figure show the widths of the 20 segments of both wires. The rectangular blocks on the left and in the middle have area $10d_1$ and $10d_2$, *i.e.*, the scale is such that the total shaded area is proportional to the $L(d_1 + d_2) + \sum l_i x_i$.

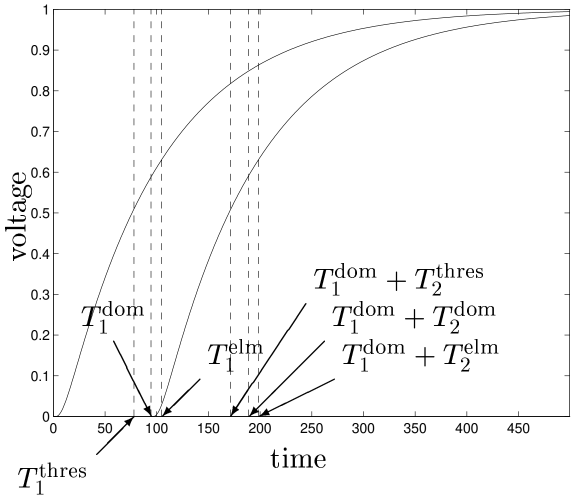

Figure 12: *Step responses for solution (a).* The figure shows the step response at the last node of the first wire, assuming that the output of the first driver goes up at $t = 0$, and the step response at the last node of the second wire assuming that the output of the second driver goes up at $t = T_1^{\mathrm{dom}}$.

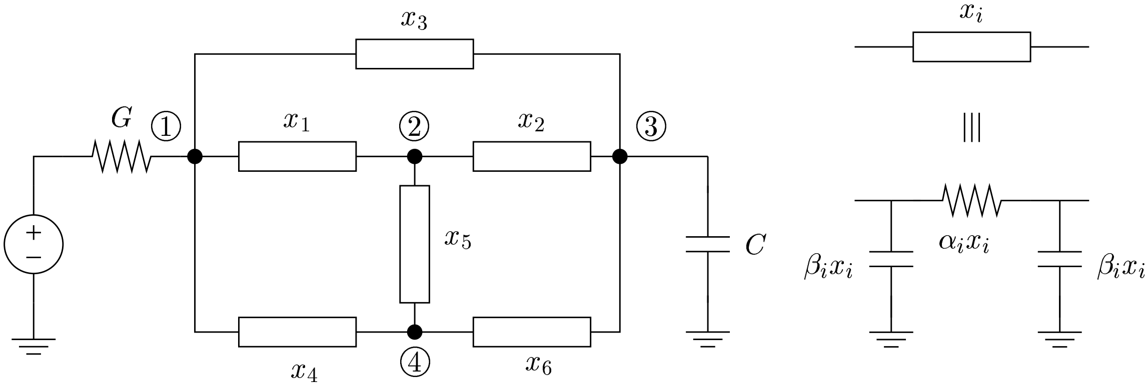

Figure 13: Interconnect network with 4 nodes, connected by 6 wire segments, shown as rectangles. The wire segments are modeled as π-segments of length l_i and width x_i, shown at right. Note that only 3 wire segments are required to connect the 4 nodes; the 6 wire segments include 3 loops.

5.3 Wire sizing and topology design

In the third example we size the wires for an interconnect circuit with four nodes, as shown in Figure 13. This example illustrates two important extensions. First, the topology of the circuit is more complex; the wires do not even form a tree. As a result, conventional Elmore delay minimization, based on geometric programming, cannot be applied. (Elmore delay minimization for circuits with meshes yields hard non-convex optimization problems.) Secondly, we will use this example to illustrate that, to a certain extent, convex optimization can be used to design the topology of interconnections. Note that this is an example of a grounded capacitor RC circuit.

The numerical values of the parameters are:

$$G = 0.1, \quad C = 10, \quad \beta_1 = \beta_2 = 10, \quad \beta_3 = 100, \quad \beta_4 = \beta_5 = 1, \quad \alpha_i = 1.0, \quad l_i = 1.$$

Since we take $l_i = 1$, the area of the circuit is simply $\sum_{i=1}^{6} x_i$.

Figure 14 shows the optimal tradeoff curve between area and dominant time constant. In this example the tradeoff curve has interesting structure, with three 'regions' that correspond to different interconnect topologies (see below).

Figure 15 shows the solution for the three points marked on the tradeoff curve. The left figures show the circuit, with the optimal width mentioned above each segment (and segments with zero width not shown). The interpretation of the third solution requires some explanation. The optimal values of the widths are $x_3 = 0.027$ and $x_i = 0$ for $i \neq 3$, which means that all conductances and capacitances connected to node 4 are zero. The interpretation of this solution poses no problem: we can simply delete node 4 from the

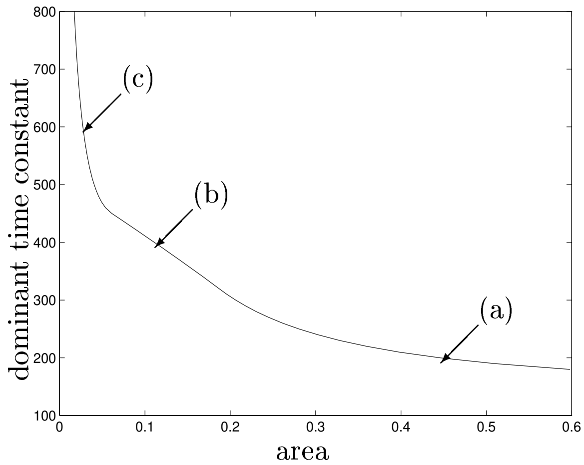

Figure 14: *Tradeoff curve.* Optimal tradeoff between area and dominant time constant for the circuit in Figure 13. The solutions at the three points marked (a), (b), (c) are given in Figure 15.

circuit. Note however that the conductance and capacitance matrices are both singular:

$$G = \begin{bmatrix} 0.127 & 0.000 & -0.027 & 0.000 \\ 0.000 & 0.000 & 0.000 & 0.000 \\ -0.027 & 0.000 & 0.027 & 0.000 \\ 0.000 & 0.000 & 0.000 & 0.000 \end{bmatrix}, \quad C = \mathbf{diag}\left(\begin{bmatrix} 2.727 & 0.000 & 12.727 & 0.000 \end{bmatrix}\right),$$

and therefore the assumptions we made in §2 do not hold. In particular, the equation $\det(\lambda C + G) = 0$ has an infinite number of solutions, so the number of eigenvalues of the pencil $(G, -C)$ is infinite. However, the dominant time constant

$$T^{\rm dom} = \min\{T \mid TG - C \geq 0\}$$

is still well defined, and yields $T^{\rm dom} = 600$. We will discuss the case of singular G or C in more detail in Appendix A.

The right half of Figure 15 shows the step responses at the different nodes, and the values of the dominant time constant and the critical Elmore delay (the Elmore delay at node 3). We can observe that the critical Elmore delay and the dominant time constant are quite close, and that the dominant time constant is a reasonable approximation for the 50%-threshold delay at the output node.

Note also the interesting fact that for design (b), the interconnect circuit has loops, which is certainly not a conventional design. Nevertheless this circuit has smaller area than any loop-free design with the same dominant time constant.

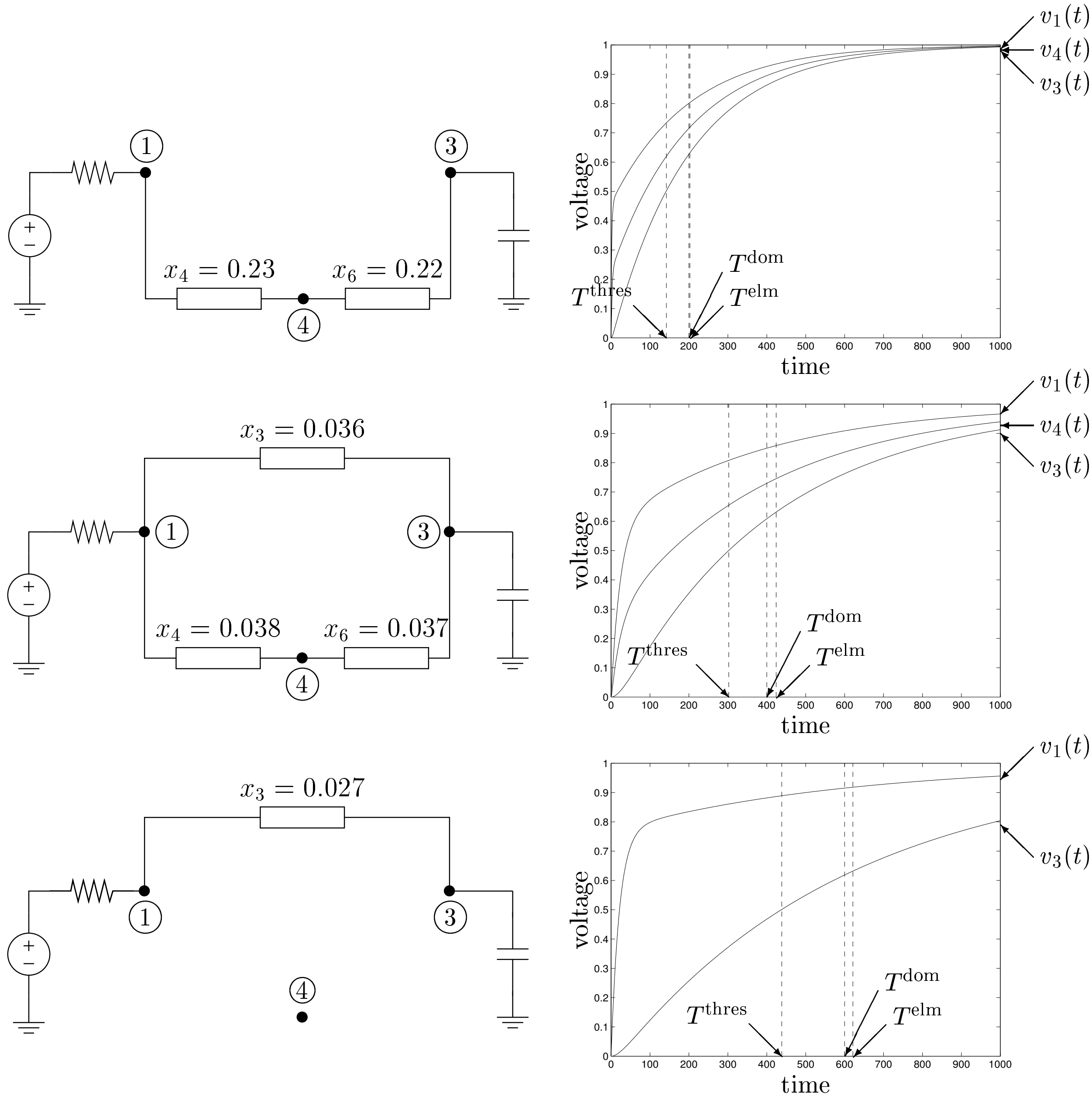

Figure 15: *Solutions.* The solutions at the three points marked on the tradeoff curve (top: solution (a), middle: solution (b), bottom: solution (c)). The left figures show the circuit with the optimal segment widths x_i. The segments that are not shown have width zero. The right figure shows the step responses at the different nodes. The vertical lines give the values of the dominant time constant T^{dom}, the Elmore delay T^{elm} at the output node, and the 0.5-threshold delay T^{thres}, at the output node 3.

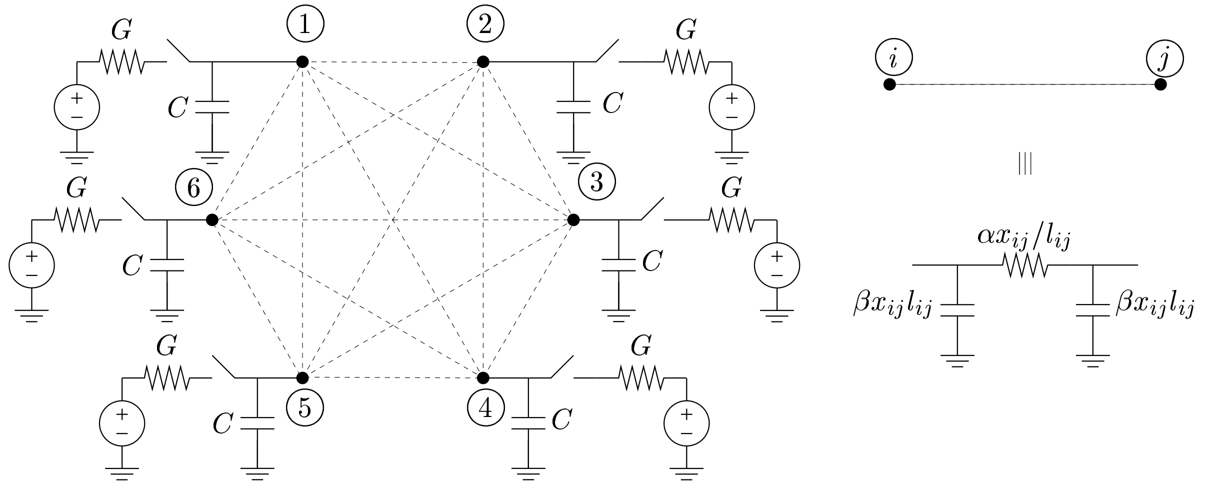

Figure 16: *Tri-state bus sizing and topology design.* The circuit on the left represents a tri-state bus connecting six nodes. Each pair of nodes is connected through a wire, shown as a dashed line, modeled as a π segment shown at right. Note that we have *fifteen* wires connecting the nodes, whereas only *five* are needed to connect them. In this example, as in the previous example, we will use dominant time constant optimization to determine the topology of the bus as well as the optimal wire sizes x_{ij}: optimal x_{ij}'s which are zero correspond to unused wires. The bus can be driven from any node. When node i drives the bus, the ith switch is closed and the others are all open.

5.4 Tri-state bus sizing and topology design

In this example we optimize a tri-state bus connecting six nodes. The example will again illustrate that dominant time constant minimization can be used to (indirectly) design the optimal topology of a circuit.

The model for the bus is shown in Figure 16. Each pair of nodes is connected by a wire (shown as a dashed line), which is modeled as a π-segment, as shown at right in the figure. (Since in the optimal designs many of the wire segments will have width zero, it is perhaps better to think of the fifteen segments as *possible* wire segments.) The capacitance and the conductance of the wire segment between node i and node j depend on its physical dimensions, *i.e.*, on its length l_{ij} and width x_{ij}: the conductance is proportional to x_{ij}/l_{ij}; the capacitance is proportional to $x_{ij}l_{ij}$. The lengths of the wires are given; the widths will be our design variables. The total wire area is $\sum_{i>j} l_{ij}x_{ij}$.

The bus can be driven from any node. When node i drives the bus, the ith switch is closed and the others are all open. Thus we really have six different circuits, each corresponding to a given node driving the bus. To characterize the threshold or Elmore delay of the bus we need to consider 36 different delays: the delay to node i when node j acts as driver. We are interested in the largest of these 36 delays, *i.e.*, the delay for the worst drive/receive pair. To constrain the dominant time constant, we require that the dominant time constant of each of the six drive configuration circuits has dominant time constant less than $T^{\max}$. In

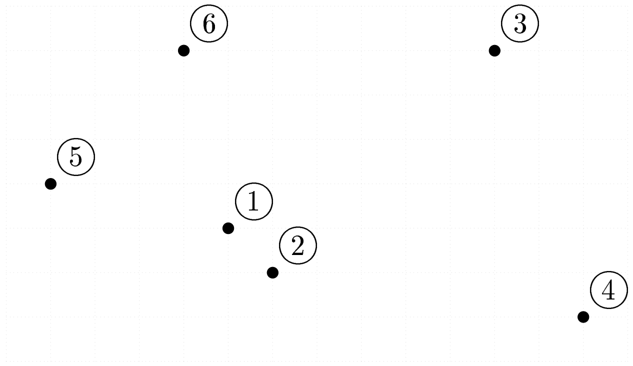

Figure 17: *Position of the six nodes.* The length l_{ij} of the wire between each two nodes i and j in Figure 16 is the ℓ_1-distance (Manhattan-distance) between the points i and j in this figure. The squares in the grid have unit size.

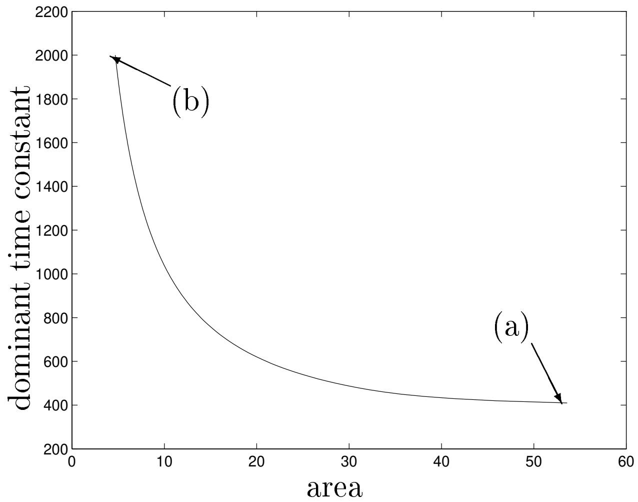

Figure 18: *Area-delay tradeoff.*

other words, if T_i^{dom} is the dominant time constant of the RC-circuit obtained by closing the switch at node i and opening the other switches, then $T^{\mathrm{dom}} = \max_i T_i$ is the measure of dominant time constant for the tri-state bus.

The numerical values used in the calculation are:

$$G = 1, \quad C = 10, \quad \beta = 0.5, \quad \alpha = 1.$$

The wire sizes are limited to a maximum value of 1.0. We assume that the geometry of the bus is as in Figure 17, and that the length l_{ij} of the wire between nodes i and j is given by the ℓ_1-distance (Manhattan distance) between points i and j in Figure 17.

Figure 18 shows the tradeoff curve between maximum dominant time constant T^{dom} and the bus area. This tradeoff curve was computed by solving the following SDP for a sequence

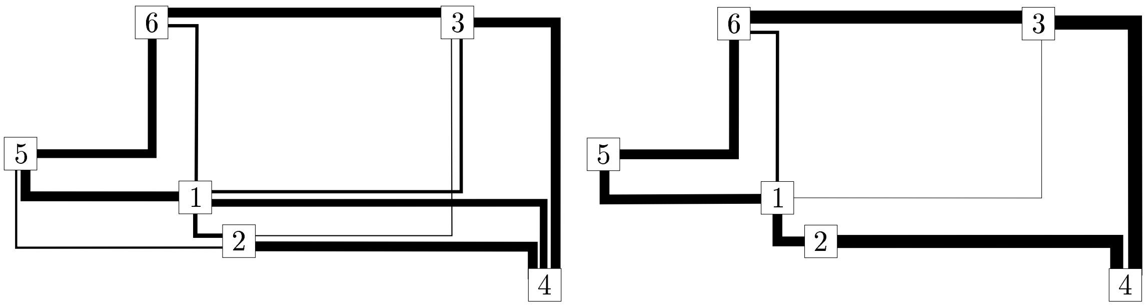

Figure 19: *Solutions marked on the tradeoff curve.* The left figure shows the line widths for solution (a). The thickness of the lines is proportional to x_{ij}. The size of the wires between (1,5), (2,4), (3,4) and (3,6) is equal to the maximum allowed value of one. There is no connection between node pairs (2,6), (3,5), (4,5) and (4,6). The right figure is the solution marked (b) on the tradeoff curve. The thickest connection is between nodes (3,4) and has width 0.14. Again all connections are drawn with a thickness proportional to their width x_{ij}. In this solution the connections between (1,4), (2,3), (2,5), (2,5), (2,6), (3,5), (4,5) and (4,6) are absent. (Note when comparing both figures, that a different scale was used for the widths in both figures. The sizes in the right figure are roughly seven times smaller than in the left figure.)

of values of $T_{\max}$:

$$\begin{array}{ll} \text{minimize} & \sum_{i>j} l_{ij} x_{ij} \\ \text{subject to} & 0 \leq x_{ij} \leq 1 \\ & T_{\max}(\tilde{G}(x) + GE_{kk}) - C(x) \geq 0, \quad k = 1, \ldots, 6. \end{array}$$

Here x denotes the vector with components x_{ij} (in any indexing order), $\tilde{G}(x)$ denotes the conductance matrix of the circuit when all switches are open, and $C(x)$ is the diagonal matrix with as its ith element the total capacitance at node i. The matrix E_{kk} is zero except for the kth diagonal element, which is equal to one. The six different LMI constraints in the above SDP correspond to the six different RC-circuits we have to consider. The conductance matrix for the circuit with switch k closed is $\tilde{G}$ with G added to its kth diagonal element, so the kth LMI constraint states that the dominant time constant of the circuit with switch k closed is less than $T_{\max}$.

Figure 19 shows the optimal widths for the two solutions marked (a) and (b) on the tradeoff curve. The connections in the figure are drawn with a thickness proportional to x_{ij}. (Note however that the scales are not the same in the left and right figure.) Note again that the topology of both designs are different: Solution (a), which is faster, uses more connections than solution (b). Also note that in both cases the optimal topologies have loops.

Figure 20 shows all step responses for both solutions. The results confirm what we expect. The smallest delay arises when the input node is 1 or 2 (the two top rows in the figure), since they lie in the middle. The delay is larger when the input node is one of the four other nodes. Note that, in both solutions, T^{dom} is equal in four of the six cases.

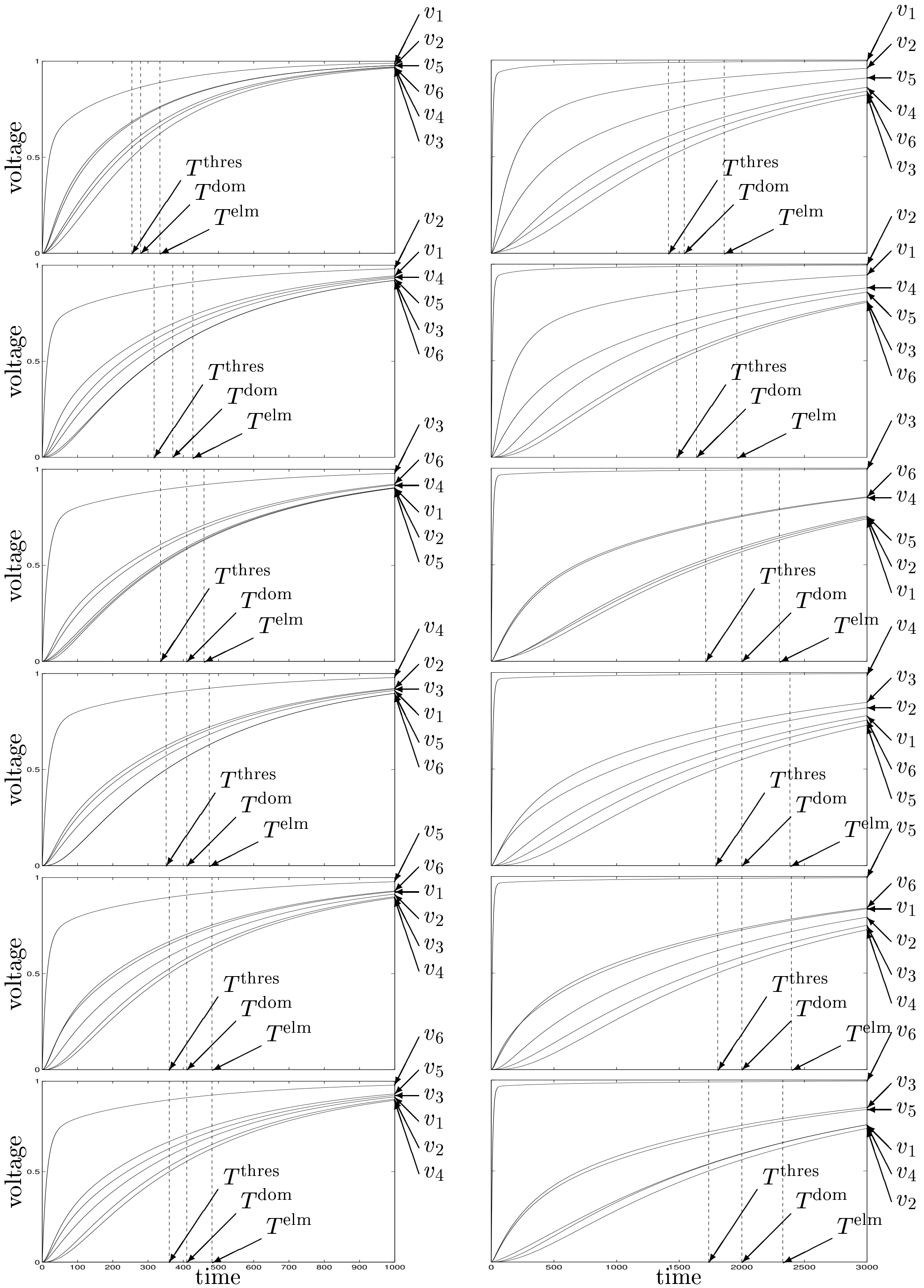

Figure 20: *Step responses.* Step responses for solution (a) (left) and solution (b) (right). The figures in the top row are the step responses when switch 1 is closed, the second row shows step responses when switch 2 is closed, etc. Each plot gives the step responses at the six different nodes of the circuit. We also indicate the values of the dominant time constant, the critical Elmore delay, and the critical 50%-threshold delay.

Again the Elmore delay is slightly higher than dominant time constant and the dominant time constant is roughly equal to the 50%-threshold delay.

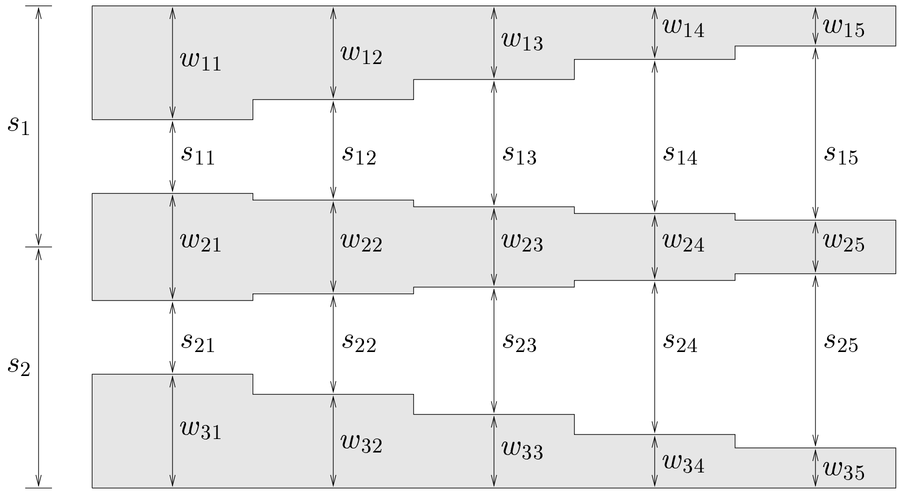

Figure 21: *Wire sizing and spacing.* Three parallel wires consisting of five segments each. The conductance and capacitance of the jth segment of wire i is proportional to w_{ij}. There is a capacitive coupling between the ith segments of wires 1 and 2, and between the ith segments of wires 2 and 3, and the value of this parasitic capacitance is inversely proportional to s_{1i}, and s_{2i}, respectively. The optimization variables are the 15 segment widths w_{ij} and the distances s_1 and s_2.

5.5 Combined wire sizing and spacing

The examples so far involved grounded capacitor RC circuits. This section will illustrate an important advantage of dominant time constant minimization over techniques based on Elmore delay: the ability to take into account non-grounded capacitors.

The problem is to determine the optimal sizes of interconnect wires *and* the optimal distances between them. We will consider an example with three wires, each consisting of five segments, as shown in Figure 21. The optimization variables are the widths w_{ij}, and the distances s_1 and s_2 between the wires.

The RC model of the three wires is shown in Figure 22. The wires are connected to a voltage source with output conductance G at one end, and to capacitive loads at the other end. As in the previous examples, each segment is modeled as a π-segment, with conductance and capacitance proportional to the segment width w_{ij}. The difference with the models used above is that we include a parasitic capacitance between the wires. We assume that there is a capacitance between the jth segments of wires 1 and 2, and between the jth segments of wires 2 and 3, with total values inversely proportional to the distances s_{1j} and s_{2j}, respectively. To obtain a lumped model, we split this distributed capacitance over two capacitors: the capacitance between segments j of wires 1 and 2 is lumped in two capacitors with value γ/s_{1j}, placed between nodes j and $j+6$, and between nodes $j+1$ and $j+7$, resp; the total capacitance between segments j of wires 2 and 3 is lumped in two capacitors with value γ/s_{2j}, placed between nodes $j+6$ and $j+12$, and between nodes $j+7$

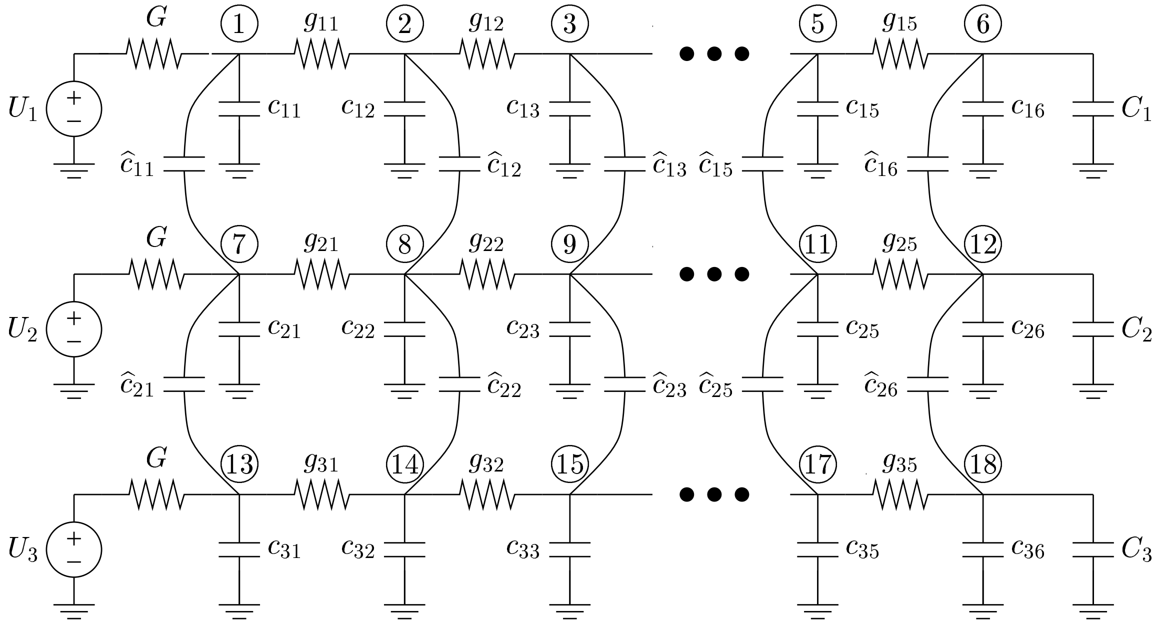

Figure 22: *RC model of the three wires shown in Figure 21.* The wires are connected to voltage sources with output conductance G at one end, and to load capacitors C_i at the other end. The conductances g_{ij} and capacitances c_{ij} are part of the π-models of the wire segments. The capacitances $\widehat{c}_{ij}$ model the capacitive coupling. The conductances and capacitances depend on the geometry of Figure 21 in the following way: $g_{ij} = \alpha w_{ij}$, $c_{i1} = \beta w_{i1}$, $c_{ij} = \beta(w_{ij} + w_{i(j-1)})$ $(1 < j < 6)$, $c_{i6} = \beta w_{i5}$, $\widehat{c}_{i1} = \gamma / s_{i1}$, $\widehat{c}_{ij} = \gamma / s_{ij} + \gamma / s_{i(j-1)}$ $(1 < j < 6)$, $\widehat{c}_{i6} = \gamma / s_{i5}$.

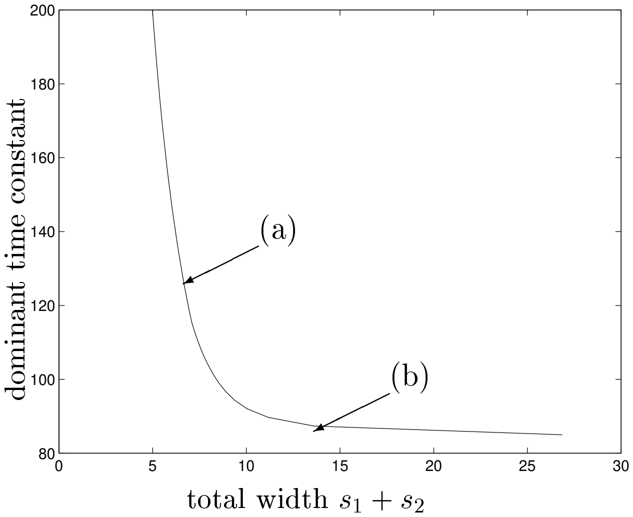

Figure 23: *Tradeoff curve.* The two objectives are the dominant time constant of the circuit and the total width $s_1 + s_2$. subject to a lower bound of 1.0 on the distances s_{ij}, and an upper bound of 2.0 on the segment widths w_{ij}.

and $j + 13$, respectively. This leads to the RC circuit in Figure 22 with, for $i = 1, 2, 3$,

$$g_{ij} = \alpha w_{ij}, \quad c_{i1} = \beta w_{i1}, \quad c_{ij} = \beta(w_{ij} + w_{i(j-1)}) \; (1 < j < 6), \quad c_{i6} = \beta w_{i5},$$

and, for $i = 1, 2$,

$$\widehat{c}_{i1} = \frac{\gamma}{s_{i1}}, \quad \widehat{c}_{ij} = \frac{\gamma}{s_{ij}} + \frac{\gamma}{s_{i(j-1)}} \; (1 < j < 6), \quad \widehat{c}_{i6} = \frac{\gamma}{s_{i5}}.$$

In the calculations we will use the numerical values

$$G = 100, \quad C_1 = 10, \quad C_2 = 20, \quad C_3 = 30, \quad \alpha = 1, \quad \beta = 0.5, \quad \gamma = 2.$$

We also impose the constraints that the distances s_{ij} between the wires must exceed 1.0, and that wire widths are less than 2.0.

Figure 10 shows the tradeoff between the total width $s_1 + s_2$ of the three wires, and the dominant time constant of the circuit. Each point on the tradeoff curve is the solution of an optimization problem

$$\begin{array}{ll} \text{mimimize} & s_1 + s_2 \\ \text{subject to} & T_{\max} G(w_{11}, \ldots, w_{35}) - C(w_{11}, \ldots, w_{35}, s_{11}, \ldots, s_{25}) \geq 0 \\ & s_{1j} = s_1 - w_{1j} - 0.5 w_{2j}, \;\; j = 1, \ldots, 5 \\ & s_{2j} = s_2 - w_{3j} - 0.5 w_{2j}, \;\; j = 1, \ldots, 5 \\ & s_{ij} \geq 1, \;\; i = 1, 2, \;\; j = 1, \ldots, 5, \\ & w_{ij} \leq 2, \;\; i = 1, 2, 3, \;\; j = 1, \ldots, 5, \end{array} \qquad (22)$$

in the variables s_1, s_2, w_{ij}, s_{ij}. Note that the capacitance matrix contains terms that are inversely proportional to the variables s_{ij}, and therefore problem (22) is *not* an SDP.

However, it can be reformulated as an SDP in the following way. First we introduce new variables $t_{ij} = 1/s_{ij}$, and write the problem as

$$\begin{array}{ll} \text{mimimize} & s_1 + s_2 \\ \text{subject to} & T_{\max} G(w_{11}, \ldots, w_{35}) - C(w_{11}, \ldots, w_{35}, t_{11}, \ldots, t_{25}) \geq 0 \\ & 1/t_{1j} \leq s_1 - w_{1j} - 0.5 w_{2j}, \quad j = 1, \ldots, 5 \\ & 1/t_{2j} \leq s_2 - w_{3j} - 0.5 w_{2j}, \quad j = 1, \ldots, 5 \\ & 0 \leq t_{ij} \leq 1, \; i = 1, 2, \quad j = 1, \ldots, 5. \end{array} \tag{23}$$

Note that we replace the equalities in the second and third constraints by inequalities. We first argue that this can be done without loss of generality. Suppose (s_i, w_{ij}, t_{ij}) are feasible in (23) with a certain objective value, and that one of the of the nonlinear inequalities in t_{ij}, *e.g.*, the inequality

$$1/t_{1j} \leq s_1 - w_{1j} - 0.5 w_{2j}$$

is not tight. Decreasing t_{1j} increases the smallest eigenvalue of the matrix $G - T_{\max} C$. (This is readily shown from the Courant-Fischer minimax theorem. It is also quite intuitive: reducing coupling decreases the dominant time constant.) Therefore we can replace t_{1j} by the value

$$\tilde{t}_{1j} = 1/(s_1 - w_{1j} - 0.5 w_{2j}),$$

while still retaining feasibility in (23), and without changing the objective value. Without loss of generality we can therefore assume that at the optimum the second and third constraints in (23) are tight. Hence problem (23) is equivalent to (22).

Problem (23) is convex in the variables s_1, s_2, t_{ij}, w_{ij}: the first constraint is an LMI; the fourth constraint is a set of linear inequalities; the second and third constraints are nonlinear convex constraints that can be cast as 3×3-LMIs by the following equivalence:

$$\begin{aligned} x \geq 0, \quad xy \geq 1 \quad & \Longleftrightarrow \quad x \geq 0, \quad \left\| \begin{bmatrix} 2 \\ x - y \end{bmatrix} \right\| \leq x + y \\ & \Longleftrightarrow \quad x \geq 0, \quad \begin{bmatrix} x + y & 0 & 2 \\ 0 & x + y & x - y \\ 2 & x - y & x + y \end{bmatrix} \geq 0. \end{aligned}$$

Figures 24 through 26 illustrate the solution marked (a) on the tradeoff curve, *i.e.*, a solution with large dominant time constant and small area. The thickest wire is number three, since it drives the largest load, the thinnest wire is number one, which drives the smallest load. Note that although the wires clearly taper off toward the end, there is a very slight increase in the width of wires 1 and 3 at segments 2 and 3. We also see that the smallest distance between the wires is equal to its minimum allowed value of 1.0, which means that the cross-coupling did not affect the optimal spacing between the wires. Figure 25 shows the output voltages for steps applied to one of the wires, while the two other input voltages remains zero. In Figure 26 we show the effect of applying a step simultaneously at two inputs, while the third input voltage remains zero.

Figures 27 through 29 illustrate the solution (b), *i.e.*, a circuit with small dominant time constant and large area.. Note that here the distance between the second and third wires is

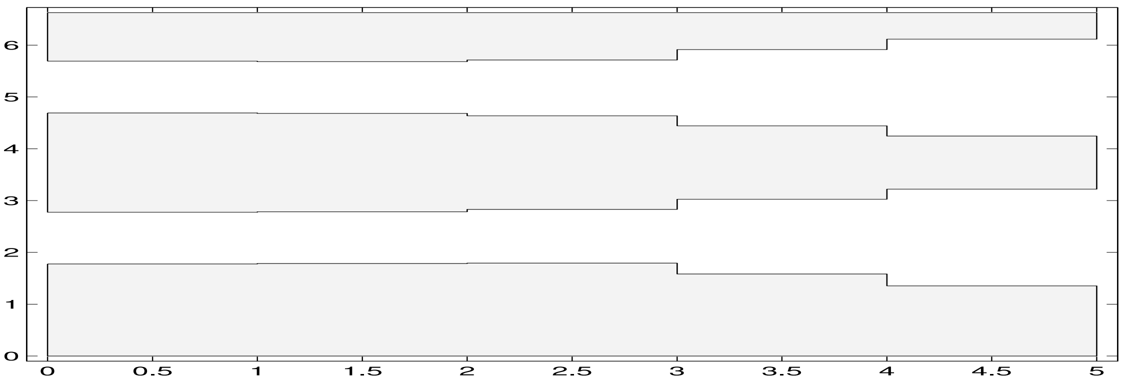

Figure 24: *Solution marked (a) on the tradeoff curve.* Note that the distance between the wires is equal to its minimal allowed value of 1.0

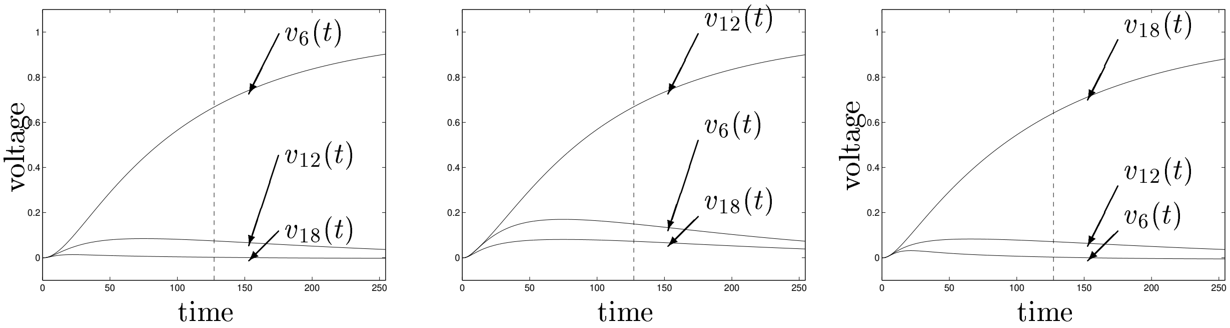

Figure 25: *Responses for solution (a).* The voltages at the output nodes due to a step applied to the first wire (left figure), second wire (center), or third wire (right). The dashed line marks the dominant time constant.

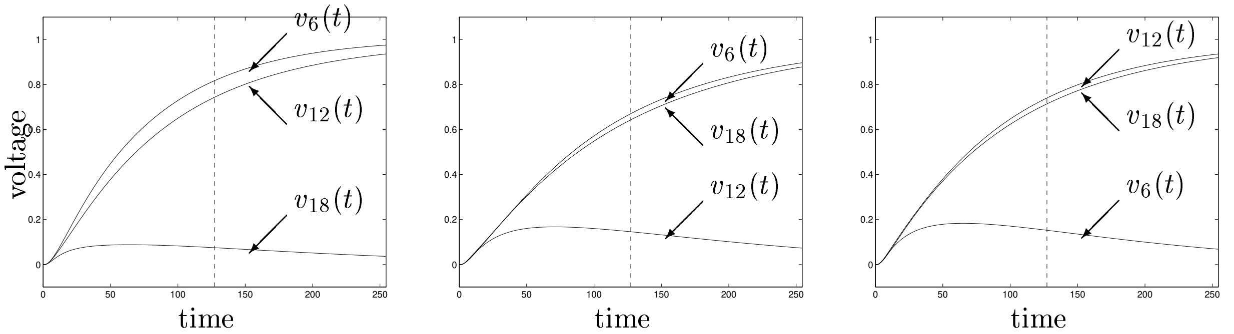

Figure 26: *Responses for solution (a).* Voltages at output nodes when a step is applied simultaneously at wires 1 and 2 (left figure), wires 1 and 3 (center), and wires 2 and 3 (right). The dashed line marks the dominant time constant.

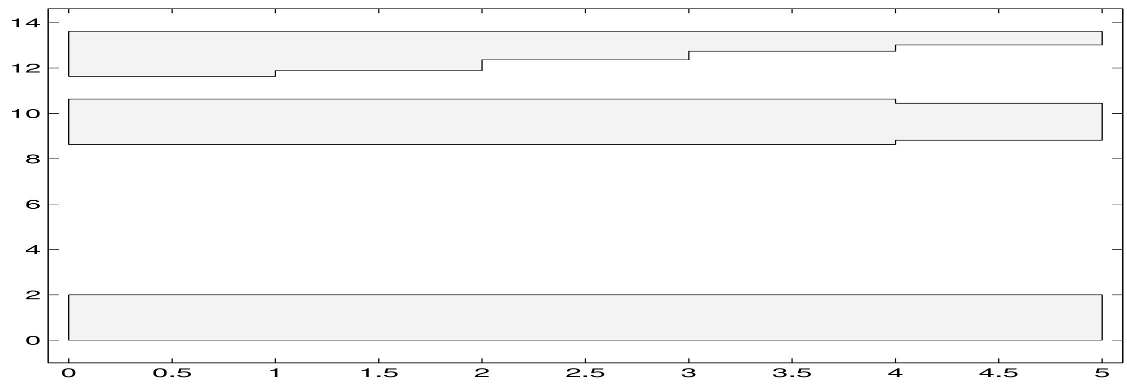

Figure 27: *Solution marked (b) on the tradeoff curve.*

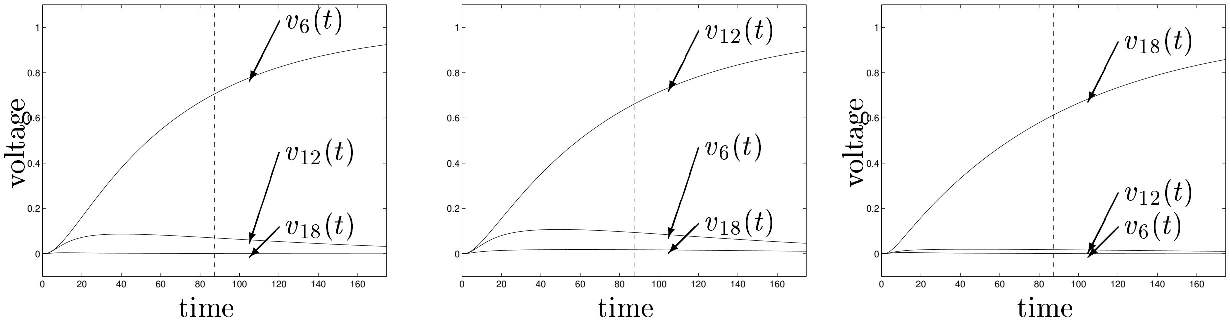

Figure 28: *Responses for solution (b).* The voltages at the output nodes, due to to a step applied to the first wire (left figure), second wire (center), or third wire (right). The dashed line marks the dominant time constant.

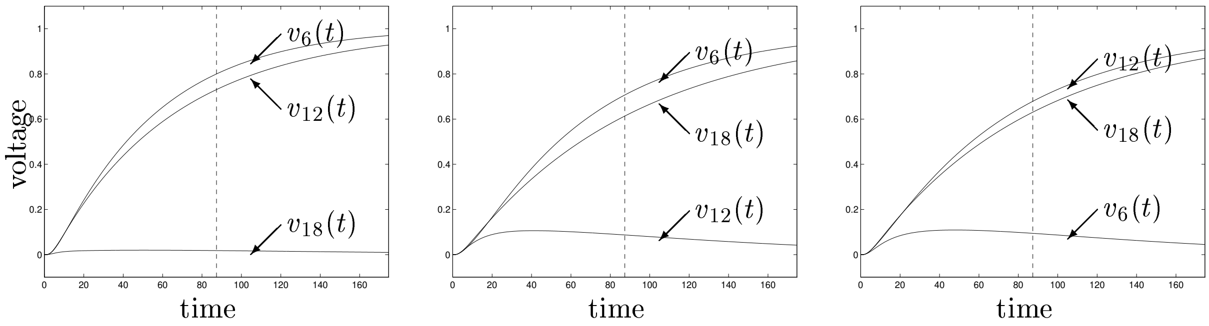

Figure 29: *Responses for solution (b).* Voltages at output nodes when a step is applied simultaneously at wires 1 and 2 (left figure), wires 1 and 3 (center), and wires 2 and 3 (right). The dashed line marks the dominant time constant.

larger than the minimum allowed value of 1.0. The other figures show the output voltages for the same situations as above.

Note that we can not guarantee that the peak due to crosstalk stays under a certain level. This would be a specification in practice, but it is difficult to incorporate into the optimization problem. However we influence the level indirectly: minimizing the dominant time constant makes the cross-talk peak shorter in time (since the dominant time constant determines how fast all voltages settle around their steady-state value). Indirectly, this also tends to make the magnitude of the peak smaller (as can be seen by comparing the crosstalk levels for the two solutions in the examples).

A practical heuristic based on the dominant time constant minimization that would guarantee a given peak level is as follows. We first solve a problem as above, *i.e.*, minimize area subject to a constraint on the dominant time constant. Then we simulate to see if crosstalk level is acceptable. If not, we increase the spacing of the wires until it is. Then we determine the optimal wire sizes again, keeping the wires at least at this minimum distance. This iteration is continued until it converges. The dominant time constant of the final result will be at least as good as the first solution and the cross talk level will not exceed the maximum level.

6 Some relations between the delay measures

In this section we derive several bounds between the three delay measures. The results allow us to translate upper bounds on T^{dom} into upper bounds on Elmore delay and threshold delays. Some of the bounds will turn out to be quite conservative. As the examples of previous section show, the 50% threshold delay, the Elmore delay, and the dominant time constant are much closer in practice than the bounds derived here would suggest.

Bounds on node voltages

We start by rewriting (7) as

$$v(t) = e^{-C^{-1}Gt}v(0) = C^{-1/2}e^{-C^{-1/2}GC^{-1/2}t}C^{1/2}v(0),$$

and use the second form to derive an upper bound on $\|v(t)\|_\infty$:

$$\begin{aligned}
\|v(t)\|_\infty &= \left\|C^{1/2}e^{-C^{-1/2}GC^{-1/2}t}C^{-1/2}v(0)\right\|_\infty \\
&\leq \left\|C^{1/2}\right\|_\infty \left\|e^{-C^{-1/2}GC^{-1/2}t}\right\|_\infty \left\|C^{-1/2}\right\|_\infty \|v(0)\|_\infty \\
&\leq \sqrt{n}\kappa_\infty(C^{1/2}) \left\|e^{-C^{-1/2}GC^{-1/2}t}\right\| \|v(0)\|_\infty \\
&= \sqrt{n}\kappa_\infty(C^{1/2}) \|v(0)\|_\infty \, e^{-t/T^{\mathrm{dom}}},
\end{aligned} \tag{24}$$

where the condition number κ_∞ is defined as $\kappa_\infty(A) = \|A\|_\infty \|A^{-1}\|_\infty$, and $\|A\|$ denotes the spectral norm of A, *i.e.*, its largest singular value. The first inequality follows from the submultiplicative property of the matrix norm ($\|AB\|_\infty \leq \|A\|_\infty \|B\|_\infty$) and the definition of the infinity-induced matrix norm ($\|Ax\|_\infty \leq \|A\|_\infty \|x\|_\infty$). The second inequality follows from the relation between the infinity-induced and the spectral norm of a matrix ($\|A\|_\infty \leq \sqrt{n}\|A\|$ for $A \in \mathbf{R}^{m\times n}$). In the last line we used the fact the largest eigenvalue of the symmetric matrix $e^{-C^{-1/2}GC^{-1/2}t}$ is $e^{-t/T^{\mathrm{dom}}}$, and that the largest eigenvalue and the spectral norm of a positive definite symmetric matrix coincide.

Note that for diagonal $C = \mathbf{diag}(C_1, \ldots, C_n)$ we have $\kappa_\infty(C^{1/2}) = (\max_i C_i)^{1/2}/(\min_j C_j)^{1/2}$.

For grounded capacitor RC circuits with $v(0) > 0$ we can also derive a lower bound on $\|v(t)\|_\infty$. Recall that for a grounded capacitor RC circuit the matrix $e^{-C^{-1}Gt}$ is elementwise nonnegative. We therefore have

$$\max_k v_k(t) = \max_k \left(e_k^T e^{-C^{-1}Gt} v(0)\right) \geq v_{\min}(0) \max_k \left(e_k^T e^{-C^{-1}Gt} e\right) \geq v_{\min}(0) e^{-t/T^{\mathrm{dom}}}, \qquad (25)$$

where $v_{\min}(0)$ is the smallest component of $v(0)$. The last inequality follows from the Gershgorin disk theorem [GL89, p. 341], which, together with the elementwise nonnegativity, implies that the eigenvalues of the matrix $e^{-C^{-1}Gt}$ are bounded above by largest row sum $\max_k e_k^T e^{-C^{-1}Gt} e$. In a grounded-capacitor RC tree we can assume $v(0) = e$ and therefore

$$\max_k v_k(t) \geq e^{-t/T^{\mathrm{dom}}}. \qquad (26)$$

Threshold delay and dominant time constant

From (24) we see that for $t \geq T^{\mathrm{dom}} \log\left(\sqrt{n}\kappa_\infty(C^{1/2})\frac{\|v(0)\|_\infty}{\alpha}\right)$, we have $\|v(t)\|_\infty \leq \alpha$, so we conclude

$$T^{\mathrm{thres}} \leq T^{\mathrm{dom}} \log\left(\sqrt{n}\kappa_\infty(C^{1/2})\frac{\|v(0)\|_\infty}{\alpha}\right).$$

In a similar way, we can derive from (25) the lower bound

$$T^{\mathrm{thres}} \geq T^{\mathrm{dom}} \log\left(\frac{v_{\min}(0)}{\alpha}\right) \qquad (27)$$

on the critical threshold delay of a grounded capacitor RC circuit. If $v(0) = e$, one obtains

$$T^{\mathrm{thres}} \geq T^{\mathrm{dom}} \log(1/\alpha)$$

Dominant time constant and Elmore delay

From (24) we have for each k

$$\begin{aligned} T_k^{\mathrm{elm}} = \int_0^\infty v_k(t)\, dt &\leq \sqrt{n}\kappa_\infty(C^{1/2})\|v(0)\|_\infty \int_0^\infty e^{-t/T^{\mathrm{dom}}}\, dt \\ &= T^{\mathrm{dom}}\sqrt{n}\kappa_\infty(C^{1/2})\|v(0)\|_\infty. \end{aligned} \qquad (28)$$

Thus we have a bound between critical Elmore delay and dominant time constant. For grounded capacitor circuits we obtain the lower bound from (26):

$$T^{\mathrm{elm}} \geq T^{\mathrm{dom}} v_{\min}(0)$$

and for a grounded capacitor RC tree

$$T^{\mathrm{elm}} \geq T^{\mathrm{dom}}.$$

	T^{thres}	T^{elm}	T^{dom}
T^{thres}		$\leq T^{\text{elm}}/\alpha$	$\leq T^{\text{dom}} \log\left(\sqrt{n}\kappa/\alpha\right)$
T^{elm}	$\leq T^{\text{thres}}\sqrt{n}\kappa/\log(1/\alpha)$		$\leq T^{\text{dom}}\sqrt{n}\kappa$
T^{dom}	$\leq T^{\text{thres}}/\log(1/\alpha)$	$\leq T^{\text{elm}}$	

Table 1: *Bounds for grounded capacitor RC trees.* κ stands for $C_{\max}^{1/2}/C_{\min}^{1/2}$.

Threshold delay and Elmore delay

We have already seen that $T^{\text{thres}} \leq T^{\text{elm}}/\alpha$ when the voltage decays monotonically.

For a grounded capacitor circuit we can also put together bounds (28) and (27), which yields

$$T^{\text{elm}} \leq T^{\text{thres}}\sqrt{n}\kappa_\infty(C^{1/2})\frac{\|v(0)\|_\infty}{\log(v_{\min}(0)/\alpha)},$$

and, for a grounded capacitor RC tree,

$$T^{\text{elm}} \leq T^{\text{thres}}\sqrt{n}\kappa_\infty(C^{1/2})\frac{1}{\log(1/\alpha)}.$$

Summary

Table 1 summarizes the bounds for grounded-capacitor RC trees, for which we have a complete set of upper and lower bounds. As an illustration, we evaluate the upper and lower bounds for the RC tree of the example in §5.1. We obtain

$$T^{\text{dom}} \leq T^{\text{elm}} \leq 4.58\,\kappa_\infty(C^{1/2})\,T^{\text{dom}}.$$

The lower bound turns out to be quite close ($T^{\text{elm}} \approx T^{\text{dom}} + 67$ over the entire range of computed values of T^{dom}). The upper bound however turns out to be very conservative (it ranges from 7842 for $T^{\text{dom}} = 370$ to 8289 for $T^{\text{dom}} = 2000$). The other examples confirm this observation that the bounds of this section are sometimes quite conservative in practice.

7 Conclusions

Computational complexity of dominant time constant minimization

We conclude with some discussion of the complexity of dominant time constant minimization via semidefinite programming. For more numerical details on interior-point methods for SDP we refer to the survey papers [VB96, LO96].

Two factors determine the overall complexity: the total number of iterations and the amount of work of one iteration. It can be shown that the number of iterations to solve an SDP to a given accuracy ϵ grows at most as $O(\sqrt{n}\log(1/\epsilon))$, where n is the size of the matrix $A(x)$ in (13) [NN94]. In practice the performance is even better than suggested by this worst-case bound. The number of iterations usually lies between 5 and 50, almost independently of problem size. For practical purposes it is therefore fair to consider the total number of iterations as constant, and to regard the work per iteration as dominating the overall complexity.

Each iteration involves solving a large system of linear equations to compute search directions. Little can be said about the complexity of this computation since it largely depends on the amount of problem structure that can be exploited. If the problem has no structure, *i.e.*, if the matrices A_i in (13) are completely dense, then the cost of one iteration is $O(mn^3 + m^2n^2)$. This is the case for the general-purpose SDP software SP and SDPSOL [VB94, WB96], which were used for the numerical examples in this paper. These codes solve problems up to several hundred variables without difficulty, but become impractical for larger problems, since they do not exploit problem structure. In all practical applications, however, there is a great deal of structure that can be exploited, and specialized codes are orders of magnitude more efficient than the general-purpose software (see for a few examples, [VB95, BVG94]).

SDP problems arising in dominant time constant minimization possess two forms of sparsity that should be exploited in a specialized code. First, the capacitance and conductance matrices C and G are usually sparse matrices (indeed C is often diagonal). Secondly, each variable x_i affects only a very small number of elements of C and G (*i.e.*, the different matrices C_i and G_i in (2) are extremely sparse).

General conclusions

Fishburn and Dunlop make an interesting remark in the conclusion of their paper on the TILOS program[FD85, §10]. They address the question whether it is justified to assume perfect step inputs, or whether the program should take into account a more realistic input waveform:

> Although there exist several static timing analyzers and a transistor sizer that take into account input waveform shape, we hesitate to do so without a convexity proof in hand. If a more accurate model turns out to be non-convex, there is always the danger that the optimizer might become trapped in a local minimum that is not a global minimum, resulting in a more pessimal solution than the less acurate model.

A similar argument can be made in favor of the approach in this paper. Accurate expressions for the delay in transistor circuits are important for simulation and timing verification, and approximations based on the first few moments seem to be very well suited for this purpose (see, for example, [PR90, FF95, GGV94b, GGV94a]. For delay optimization, however, these expressions lead to complicated non-convex optimization problems, with possibly many local minima. This is already the case for the Elmore delay (the first moment of the transfer function) of a grounded capacitor RC circuit with loops of resistors. Optimizing the dominant time constant on the other hand leads to tractable convex optimization problems even in general RC circuits.

Acknowledgments

We thank Frank Wu of Intel for suggesting a tri-state bus example.

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A Singular C or G

We now come back to the assumption in §2 that the capacitance matrix C and conductance matrix G are both strictly positive definite. This assumption simplified the definition and interpretation of the dominant time constant, since it ensures that the number of generalized eigenvalues, *i.e.*, the number of roots of the polynomial $\det(\lambda C + G)$, is exactly equal to n.

In Example 3 we have encountered a case where both C and G were singular. In this case the dominant time constant minimization still leads to meaningful results, provided we do not define the dominant time constant in terms of the largest generalized eigenvalue, but use the LMI definition

$$T^{\mathrm{dom}} = \inf\{T \mid TG - C \geq 0\} \tag{29}$$

(we should add that $T^{\mathrm{dom}} = +\infty$ if there is no T with $TG - C \geq 0$). In this appendix we show that this definition is indeed meaningful and valid when C and G are only positive semidefinite, *i.e.*, possibly singular.

Given arbitrary positive semidefinite C and G, one can always change coordinates to bring the circuit equations $C\dot{v} = -Gv$ into the form

$$\begin{bmatrix} \widehat{C} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} d\widehat{v}_1/dt \\ d\widehat{v}_2/dt \\ d\widehat{v}_3/dt \end{bmatrix} = - \begin{bmatrix} \widehat{G}_{11} & \widehat{G}_{12} & 0 \\ \widehat{G}_{12}^T & \widehat{G}_{22} & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \widehat{v}_1(t) \\ \widehat{v}_2(t) \\ \widehat{v}_3(t) \end{bmatrix}, \tag{30}$$

with $\widehat{C}$ and $\widehat{G}_{22}$ strictly positive definite. Note that these equations are a combination of differential and algebraic equations.

Assume $\widehat{C} \in \mathbf{R}^{p\times p}$. The circuit equation (30) is equivalent to

$$d\widehat{v}_1/dt = -\widehat{C}^{-1}\left(\widehat{G}_{11} - \widehat{G}_{12}\widehat{G}_{22}^{-1}\widehat{G}_{12}^T\right)\widehat{v}_1(t), \quad \widehat{v}_2(t) = -\widehat{G}_{22}^{-1}\widehat{G}_{12}^T v_1(t)$$

and $v_3(t)$ completely arbitrary. Let λ_i, $i = 1, \ldots, p$, be the eigenvalues of the matrix

$$-\widehat{C}^{-1}\left(\widehat{G}_{11} + \widehat{G}_{12}\widehat{G}_{22}^{-1}\widehat{G}_{12}^T\right)$$

sorted in decreasing order. Then all solutions of (30) have the form

$$\widehat{v}_1(t) = \sum_i \alpha_i e^{\lambda_i t}, \quad \widehat{v}_2(t) = \sum_i \beta_i e^{\lambda_i t}, \quad \widehat{v}_3(t) \text{ arbitrary.}$$

The components of v_3 correspond to nodes that are not connected by capacitors or resistors to the rest of the circuit (as was the case with node 4 in Example 3). It is therefore natural to ignore v_3 when defining the dominant time constant (or, equivalently, to impose the extra assumption that $v_3(t) \equiv 0$), and to say that $T^{\mathrm{dom}} = -1/\lambda_1$ (and $T^{\mathrm{dom}} = \infty$ if $\lambda_1 = 0$).

Finally, to see that this definition coincides with (29), note that $T \geq -1/\lambda_1$ if and only if the LMI

$$\begin{bmatrix} T\widehat{G}_{11} - \widehat{C} & T\widehat{G}_{12} \\ T\widehat{G}_{12}^T & T\widehat{G}_{22} \end{bmatrix} \geq 0,$$

holds. This can be easily shown by using a Schur complement (see, *e.g.*, [VB96]).